TMS320UC5402 Fixed-Point Digital Signal Processor

Data Manual

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

REVISION HISTORY

REVISION	DATE	PRODUCT STATUS	HIGHLIGHTS
*	April 1999	Product Preview	Original
A	December 1999	Product Preview	Updated characteristic data.
B	September 2001	Production Data	Converted document to Data Manual format. Udated characteristic data.

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1 Introduction

This section describes the main features of the TMS320UC5402, lists the pin assignments, and describes the function of each pin. This data manual also provides a detailed description section, electrical specifications, parameter measurement information, and mechanical data about the available packaging.

NOTE: This data manual is designed to be used in conjunction with the *TMS320C54x™ DSP Functional Overview* (literature number SPRU307).

1.1 Features

- **Advanced Multibus Architecture With Three Separate 16-Bit Data Memory Buses and One Program Memory Bus**
- **40-Bit Arithmetic Logic Unit (ALU), Including a 40-Bit Barrel Shifter and Two Independent 40-Bit Accumulators**
- **17- × 17-Bit Parallel Multiplier Coupled to a 40-Bit Dedicated Adder for Non-Pipelined Single-Cycle Multiply/Accumulate (MAC) Operation**
- **Compare, Select, and Store Unit (CSSU) for the Add/Compare Selection of the Viterbi Operator**
- **Exponent Encoder to Compute an Exponent Value of a 40-Bit Accumulator Value in a Single Cycle**
- **Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)**
- **Data Bus With a Bus-Holder Feature**
- **Extended Addressing Mode for 1M × 16-Bit Maximum Addressable External Program Space**
- **4K x 16-Bit On-Chip ROM**
- **16K x 16-Bit On-Chip Dual-Access RAM**
- **Single-Instruction-Repeat and Block-Repeat Operations for Program Code**
- **Block-Memory-Move Instructions for Efficient Program and Data Management**
- **Instructions With a 32-Bit-Long Word Operand**
- **Instructions With Two- or Three-Operand Reads**
- **Arithmetic Instructions With Parallel Store and Parallel Load**
- **Conditional Store Instructions**
- **Fast Return From Interrupt**
- **On-Chip Peripherals**
  - **Software-Programmable Wait-State Generator and Programmable Bank Switching**
  - **On-Chip Phase-Locked Loop (PLL) Clock Generator With Internal Oscillator or External Clock Source**
  - **Two Multichannel Buffered Serial Ports (McBSPs)**
  - **Enhanced 8-Bit Parallel Host-Port Interface (HPI8)**
  - **Two 16-Bit Timers**
  - **Six-Channel Direct Memory Access (DMA) Controller**
- **Power Consumption Control With IDLE1, IDLE2, and IDLE3 Instructions With Power-Down Modes**
- **CLKOUT Off Control to Disable CLKOUT**
- **On-Chip Scan-Based Emulation Logic, IEEE Std 1149.1† (JTAG) Boundary Scan Logic**
- **12.5-ns Single-Cycle Fixed-Point Instruction Execution Time (80 MIPS)**
- **1.8-V Core Power Supply**
- **1.8-V to 3.6-V I/O Power Supply Enables Operation With a Single 1.8-V Supply or with Dual Supplies**
- **Available in a 144-Pin Low-Profile Quad Flatpack (LQFP) (PGE Suffix)**
- **Available in a 144-Ball MicroStar™ Ball Grid Array (BGA) (GGU Suffix)**

TMS320C54x and MicroStar BGA are trademarks of Texas Instruments.

† IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

1.2 Description

The TMS320UC5402 fixed-point, digital signal processor (DSP) (hereafter referred to as the UC5402 unless otherwise specified) is ideal for low-power, high-performance applications. This processor offers very low power consumption and the flexibility to support various system voltage configurations. The wide range of I/O voltage enables it to operate with a single 1.8-V power supply or with dual power supplies for mixed voltage systems. This feature eliminates the need for external level-shifting and reduces power consumption in emerging sub-3V systems.

Texas Instrument (TI) DSPs do not require specific power sequencing between the core supply and the I/O supply. However, systems should be designed to ensure that neither supply is powered up for extended periods of time if the other supply is below the proper operating voltage. Excessive exposure to these conditions can adversely affect the long-term reliability of the device.

System-level concerns such as bus contention may require supply sequencing to be implemented. In this case, the core supply should be powered up at the same time as, or prior to, the I/O buffers and powered down after the I/O buffers.

The UC5402 is based on an advanced modified Harvard architecture that has one program memory bus and three data memory buses. This processor provides an arithmetic logic unit (ALU) with a high degree of parallelism, application-specific hardware logic, on-chip memory, and additional on-chip peripherals. The basis of the operational flexibility and speed of this DSP is a highly specialized instruction set.

1.3 Pin Assignments

Figure 1–1 illustrates the ball locations for the 144-terminal ball grid array (BGA) package and is used in conjunction with Table 1–1 to locate signal names and ball grid numbers. DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU. V_{SS} is the ground for both the I/O pins and the core CPU.

1.3.1 Terminal Assignments for the GGU Package

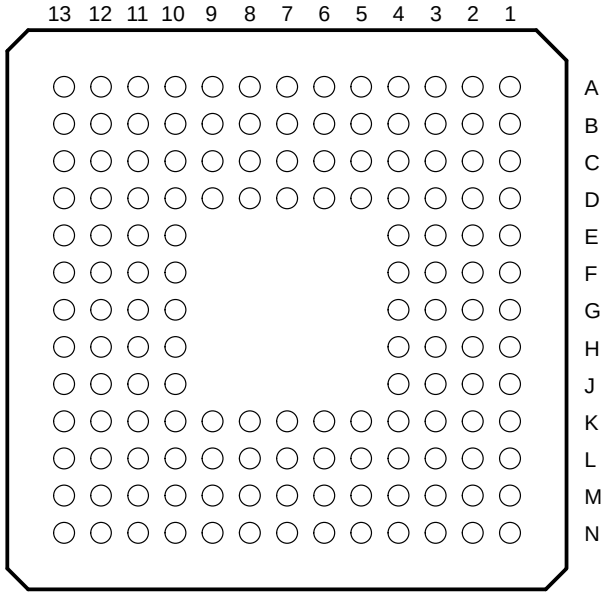


Figure 1–1. 144-Terminal GGU Ball Grid Array (Bottom View)

Table 1–1. Terminal Assignments (144-Terminal GGU Package)†

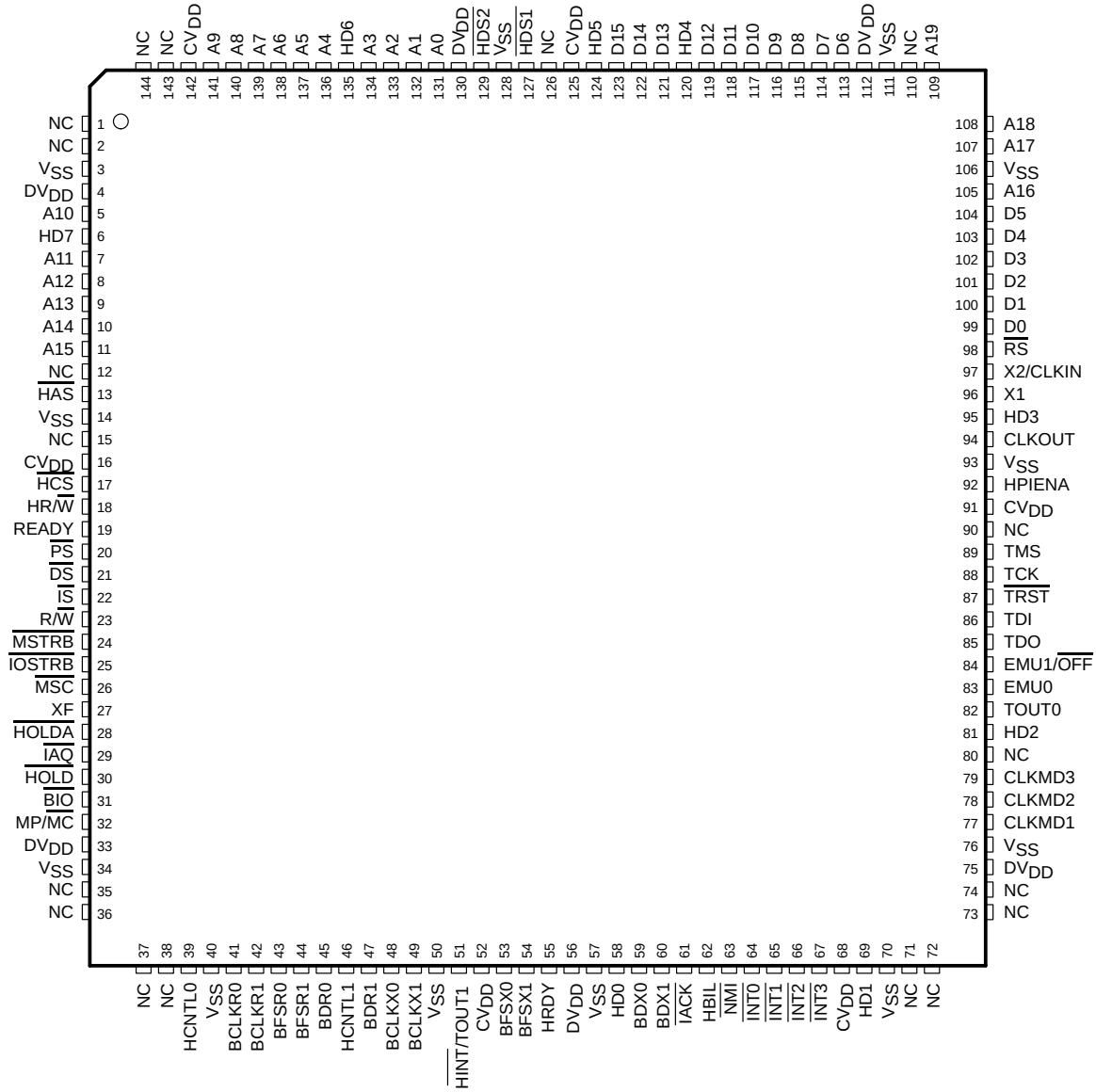
SIGNAL NAME	BGA BALL #	SIGNAL NAME	BGA BALL #	SIGNAL NAME	BGA BALL #	SIGNAL NAME	BGA BALL #
NC	A1	NC	N13	NC	N1	A19	A13
NC	B1	NC	M13	NC	N2	NC	A12
V_{SS}	C2	DV_{DD}	L12	HCNTL0	M3	V_{SS}	B11
DV_{DD}	C1	V_{SS}	L13	V_{SS}	N3	DV_{DD}	A11
A10	D4	CLKMD1	K10	BCLKR0	K4	D6	D10
HD7	D3	CLKMD2	K11	BCLKR1	L4	D7	C10
A11	D2	CLKMD3	K12	BFSR0	M4	D8	B10
A12	D1	NC	K13	BFSR1	N4	D9	A10
A13	E4	HD2	J10	BDR0	K5	D10	D9
A14	E3	TOUT0	J11	HCNTL1	L5	D11	C9
A15	E2	EMU0	J12	BDR1	M5	D12	B9
NC	E1	EMU1/$\overline{OFF}$	J13	BCLKX0	N5	HD4	A9
$\overline{HAS}$	F4	TDO	H10	BCLKX1	K6	D13	D8
V_{SS}	F3	TDI	H11	V_{SS}	L6	D14	C8
NC	F2	$\overline{TRST}$	H12	$\overline{HINT}$/TOUT1	M6	D15	B8
CV_{DD}	F1	TCK	H13	CV_{DD}	N6	HD5	A8
$\overline{HCS}$	G2	TMS	G12	BFSX0	M7	CV_{DD}	B7
HR/$\overline{W}$	G1	NC	G13	BFSX1	N7	NC	A7
READY	G3	CV_{DD}	G11	HRDY	L7	$\overline{HDS1}$	C7
$\overline{PS}$	G4	HPIENA	G10	DV_{DD}	K7	V_{SS}	D7
$\overline{DS}$	H1	V_{SS}	F13	V_{SS}	N8	$\overline{HDS2}$	A6
$\overline{IS}$	H2	CLKOUT	F12	HD0	M8	DV_{DD}	B6
R/$\overline{W}$	H3	HD3	F11	BDX0	L8	A0	C6
$\overline{MSTRB}$	H4	X1	F10	BDX1	K8	A1	D6
$\overline{IOSTRB}$	J1	X2/CLKIN‡	E13	$\overline{IACK}$	N9	A2	A5
$\overline{MSC}$	J2	$\overline{RS}$	E12	HBIL	M9	A3	B5
XF	J3	D0	E11	$\overline{NMI}$	L9	HD6	C5
$\overline{HOLDA}$	J4	D1	E10	$\overline{INT0}$	K9	A4	D5
$\overline{IAQ}$	K1	D2	D13	$\overline{INT1}$	N10	A5	A4
$\overline{HOLD}$	K2	D3	D12	$\overline{INT2}$	M10	A6	B4
$\overline{BIO}$	K3	D4	D11	$\overline{INT3}$	L10	A7	C4
MP/$\overline{MC}$	L1	D5	C13	CV_{DD}	N11	A8	A3
DV_{DD}	L2	A16	C12	HD1	M11	A9	B3
V_{SS}	L3	V_{SS}	C11	V_{SS}	L11	CV_{DD}	C3
NC	M1	A17	B13	NC	N12	NC	A2
NC	M2	A18	B12	NC	M12	NC	B2

† DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU. V_{SS} is the ground for both the I/O pins and the core CPU.

‡ If an external clock source is used, the CLKIN signal level should not exceed CV_{DD} + 0.3 V.

1.3.2 Pin Assignments for the PGE Package

The TMS320UC5402PGE 144-pin low-profile quad flatpack (LQFP) pin assignments are shown in Figure 1–2. DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU. V_{SS} is the ground for both the I/O pins and the core CPU.



NOTE A: NC = No connection. These pins should be left unconnected.

Figure 1–2. 144-Pin PGE Low-Profile Quad Flatpack (Top View)

1.4 Signal Descriptions

Table 1–2 lists each signal, function, and operating mode(s) grouped by function. See Section 1.3 for exact pin locations based on package type.

Table 1–2. Signal Descriptions

TERMINAL NAME	TYPE†	DESCRIPTION
DATA SIGNALS		
A19 (MSB) A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 (LSB)	O/Z	Parallel address bus A19 [most significant bit (MSB)] through A0 [least significant bit (LSB)]. The lower sixteen address pins (A0 to A15) are multiplexed to address all external memory (program, data) or I/O, while the upper four address pins (A16 to A19) are only used to address external program space. These pins are placed in the high-impedance state when the hold mode is enabled, or when EMU1/$\overline{\text{OFF}}$ is low.
D15 (MSB) D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 (LSB)	I/O/Z	Parallel data bus D15 (MSB) through D0 (LSB). The sixteen data pins (D0 to D15) are multiplexed to transfer data between the core CPU and external data/program memory or I/O devices. The data bus is placed in the high-impedance state when not outputting or when $\overline{\text{RS}}$ or $\overline{\text{HOLD}}$ is asserted. The data bus also goes into the high-impedance state when EMU1/$\overline{\text{OFF}}$ is low. The data bus has bus holders to reduce the static power dissipation caused by floating, unused pins. These bus holders also eliminate the need for external bias resistors on unused pins. When the data bus is not being driven by the UC5402, the bus holders keep the pins at the previous logic level. The data bus holders on the UC5402 are disabled at reset and can be enabled/disabled via the BH bit of the bank-switching control register (BSCR).
INITIALIZATION, INTERRUPT, AND RESET OPERATIONS		
$\overline{\text{IACK}}$	O/Z	Interrupt acknowledge signal. $\overline{\text{IACK}}$ Indicates receipt of an interrupt and that the program counter is fetching the interrupt vector location designated by A15–A0. $\overline{\text{IACK}}$ also goes into the high-impedance state when EMU1/$\overline{\text{OFF}}$ is low.
$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ $\overline{\text{INT3}}$	I	External user interrupts. $\overline{\text{INT0}}$–$\overline{\text{INT3}}$ are prioritized and are maskable by the interrupt mask register (IMR) and the interrupt mode bit. $\overline{\text{INT0}}$ –$\overline{\text{INT3}}$ can be polled and reset by way of the interrupt flag register (IFR).
$\overline{\text{NMI}}$	I	Nonmaskable interrupt. $\overline{\text{NMI}}$ is an external interrupt that cannot be masked by way of the INTM bit (in the ST1 register) or the IMR. When $\overline{\text{NMI}}$ is activated, the processor traps to the appropriate vector location.

† I = input, O = output, Z = high impedance, S = supply

‡ If an external clock source is used, the CLKIN signal level should not exceed CV_{DD} + 0.3 V.

Table 1–2. Signal Descriptions (Continued)

TERMINAL NAME	TYPE†	DESCRIPTION
INITIALIZATION, INTERRUPT, AND RESET OPERATIONS (CONTINUED)		
$\overline{RS}$	I	Reset. $\overline{RS}$ causes the digital signal processor (DSP) to terminate execution and causes a reinitialization of the CPU and peripherals. When $\overline{RS}$ is brought to a high level, execution begins at location 0FF80h of program memory. $\overline{RS}$ affects various registers and status bits.
MP/$\overline{MC}$	I	Microprocessor/microcomputer mode select. If active (low) at reset, microcomputer mode is selected, and the internal program ROM is mapped into the upper 4K words of program memory space. If the pin is driven high during reset, microprocessor mode is selected, and the on-chip ROM is removed from program space. This pin is only sampled at reset, and the MP/$\overline{MC}$ bit of the processor mode status (PMST) register can override the mode that is selected at reset.
MULTIPROCESSING SIGNALS		
$\overline{BIO}$	I	Branch control. A branch can be conditionally executed when $\overline{BIO}$ is active. If low, the processor executes the conditional instruction. For the XC instruction, the $\overline{BIO}$ condition is sampled during the decode phase of the pipeline; all other instructions sample $\overline{BIO}$ during the read phase of the pipeline.
XF	O/Z	External flag output (latched software-programmable signal). XF is set high by the SSBX XF instruction, set low by the RSBX XF instruction or by loading ST1. XF is used for signaling other processors in multiprocessor configurations or used as a general-purpose output pin. XF goes into the high-impedance state when EMU1/$\overline{OFF}$ is low, and is set high at reset.
MEMORY CONTROL SIGNALS		
$\overline{DS}$ $\overline{PS}$ $\overline{IS}$	O/Z	Data, program, and I/O space select signals. $\overline{DS}$, $\overline{PS}$, and $\overline{IS}$ are always high unless driven low for accessing a particular external memory space. Active period corresponds to valid address information. $\overline{DS}$, $\overline{PS}$, and $\overline{IS}$ are placed in the high-impedance state in the hold mode; the signals also go into the high-impedance state when EMU1/$\overline{OFF}$ is low.
$\overline{MSTRB}$	O/Z	Memory strobe signal. $\overline{MSTRB}$ is always high unless low-level asserted to indicate an external bus access to data or program memory. $\overline{MSTRB}$ is placed in the high-impedance state in the hold mode; it also goes into the high-impedance state when EMU1/$\overline{OFF}$ is low.
READY	I	Data ready. READY indicates that an external device is prepared for a bus transaction to be completed. If the device is not ready (READY is low), the processor waits one cycle and checks READY again. Note that the processor performs ready detection if at least two software wait states are programmed. The READY signal is not sampled until the completion of the software wait states.
R/$\overline{W}$	O/Z	Read/write signal. R/$\overline{W}$ indicates transfer direction during communication to an external device. R/$\overline{W}$ is normally in the read mode (high), unless it is asserted low when the DSP performs a write operation. R/$\overline{W}$ is placed in the high-impedance state in hold mode; it also goes into the high-impedance state when EMU1/$\overline{OFF}$ is low.
$\overline{IOSTRB}$	O/Z	I/O strobe signal. $\overline{IOSTRB}$ is always high unless low-level asserted to indicate an external bus access to an I/O device. $\overline{IOSTRB}$ is placed in the high-impedance state in the hold mode; it also goes into the high-impedance state when EMU1/$\overline{OFF}$ is low.
$\overline{HOLD}$	I	Hold. $\overline{HOLD}$ is asserted to request control of the address, data, and control lines. When acknowledged by the C54x™, these lines go into the high-impedance state.
$\overline{HOLDA}$	O/Z	Hold acknowledge. $\overline{HOLDA}$ indicates that the UC5402 is in a hold state and that the address, data, and control lines are in the high-impedance state, allowing the external memory interface to be accessed by other devices. $\overline{HOLDA}$ also goes into the high-impedance state when EMU1/$\overline{OFF}$ is low.
$\overline{MSC}$	O/Z	Microstate complete. $\overline{MSC}$ indicates completion of all software wait states. When two or more software wait states are enabled, the $\overline{MSC}$ pin goes active at the beginning of the first software wait state and goes inactive high at the beginning of the last software wait state. If connected to the READY input, $\overline{MSC}$ forces one external wait state after the last internal wait state is completed. $\overline{MSC}$ also goes into the high-impedance state when EMU1/$\overline{OFF}$ is low.
$\overline{IAQ}$	O/Z	Instruction acquisition signal. $\overline{IAQ}$ is asserted (active-low) when there is an instruction address on the address bus. $\overline{IAQ}$ goes into the high-impedance state when EMU1/$\overline{OFF}$ is low.

† I = input, O = output, Z = high impedance, S = supply

‡ If an external clock source is used, the CLKIN signal level should not exceed CV_{DD} + 0.3 V.

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Table 1–2. Signal Descriptions (Continued)

TERMINAL NAME	TYPE†	DESCRIPTION
PLL/TIMER SIGNALS		
CLKOUT	O/Z	Master clock output signal. CLKOUT cycles at the machine-cycle rate of the CPU. The internal machine cycle is bounded by the rising edges of this signal. CLKOUT also goes into the high-impedance state when EMU1/$\overline{\text{OFF}}$ is low.
CLKMD1 CLKMD2 CLKMD3	I	Clock mode-select signals. These inputs select the mode that the clock generator is initialized to after reset. The logic levels of CLKMD1–CLKMD3 are latched when the reset pin is low, and the clock mode register is initialized to the selected mode. After reset, the clock mode can be changed through software, but the clock mode-select signals have no effect until the device is reset again.
X2/CLKIN‡	I	Clock/PLL input. If the internal oscillator is not being used, the X2/CLKIN functions as the clock input.
X1	O	Output pin from the internal oscillator for the crystal. If the internal oscillator is not used, X1 should be left unconnected. X1 does not go into the high-impedance state when EMU1/$\overline{\text{OFF}}$ is low.
TOUT0	O/Z	Timer0 output. TOUT0 signals a pulse when the on-chip timer 0 counts down past zero. The pulse is a CLKOUT cycle wide. TOUT0 also goes into the high-impedance state when EMU1/$\overline{\text{OFF}}$ is low.
$\overline{\text{HINT}}$/TOUT1	O/Z	Timer1 output. TOUT1 signals a pulse when the on-chip timer 1 counts down past zero. The pulse is one CLKOUT cycle wide. The TOUT1 output is multiplexed with the $\overline{\text{HINT}}$ pin of the HPI and is only available when the HPI is disabled. TOUT1 also goes into the high-impedance state when EMU1/$\overline{\text{OFF}}$ is low.
MULTICHANNEL BUFFERED SERIAL PORT SIGNALS		
BCLKR0 BCLKR1	I/O/Z	Receive clock input. BCLKR serves as the serial shift clock for the buffered serial port receiver.
BDR0 BDR1	I	Serial data receive input
BFSR0 BFSR1	I/O/Z	Frame synchronization pulse for receive input. The BFSR pulse initiates the receive data process over BDR.
BCLKX0 BCLKX1	I/O/Z	Transmit clock. BCLKX serves as the serial shift clock for the McBSP transmitter. BCLKX can be configured as an input or an output; it is configured as an input following reset. BCLKX enters the high-impedance state when EMU1/$\overline{\text{OFF}}$ goes low.
BDX0 BDX1	O/Z	Serial data transmit output. BDX is placed in the high-impedance state when not transmitting, when $\overline{\text{RS}}$ is asserted, or when EMU1/$\overline{\text{OFF}}$ is low.
BFSX0 BFSX1	I/O/Z	Frame synchronization pulse for transmit input/output. The BFSX pulse initiates the transmit data process. BFSX can be configured as an input or an output; it is configured as an input following reset. BFSX goes into the high-impedance state when EMU1/$\overline{\text{OFF}}$ is low.
HOST-PORT INTERFACE SIGNALS		
HD0–HD7	I/O/Z	Parallel bidirectional data bus. The HPI data bus is used by a host device bus to exchange information with the HPI registers. These pins can also be used as general-purpose I/O pins. HD0–HD7 is placed in the high-impedance state when not outputting data or when EMU1/$\overline{\text{OFF}}$ is low. The HPI data bus includes bus holders to reduce the static power dissipation caused by floating, unused pins. When the HPI data bus is not being driven by the UC5402, the bus holders keep the pins at the previous logic level. The HPI data bus holders are disabled at reset and can be enabled/disabled via the HBH bit of the BSCR.
HCNTL0 HCNTL1	I	Control. HCNTL0 and HCNTL1 select a host access to one of the three HPI registers. The control inputs have internal pullup resistors that are only enabled when HPIENA = 0.
HBIL	I	Byte identification. HBIL identifies the first or second byte of transfer. The HBIL input has an internal pullup resistor that is only enabled when HPIENA = 0.
$\overline{\text{HCS}}$	I	Chip select. $\overline{\text{HCS}}$ is the select input for the HPI and must be driven low during accesses. The chip-select input has an internal pullup resistor that is only enabled when HPIENA = 0.
$\overline{\text{HDS1}}$ $\overline{\text{HDS2}}$	I	Data strobe. $\overline{\text{HDS1}}$ and $\overline{\text{HDS2}}$ are driven by the host read and write strobes to control transfers. The strobe inputs have internal pullup resistors that are only enabled when HPIENA = 0.
$\overline{\text{HAS}}$	I	Address strobe. Hosts with multiplexed address and data pins require $\overline{\text{HAS}}$ to latch the address in the HPIA register. $\overline{\text{HAS}}$ has an internal pullup resistor that is only enabled when HPIENA = 0.

† I = input, O = output, Z = high impedance, S = supply

‡ If an external clock source is used, the CLKIN signal level should not exceed CV_{DD} + 0.3 V.

Table 1–2. Signal Descriptions (Continued)

TERMINAL NAME	TYPE†	DESCRIPTION
HOST-PORT INTERFACE SIGNALS (CONTINUED)		
HR/$\overline{W}$	I	Read/write. HR/$\overline{W}$ controls the direction of an HPI transfer. HR/$\overline{W}$ has an internal pullup resistor that is only enabled when HPIENA = 0.
HRDY	O/Z	Ready. The ready output informs the host when the HPI is ready for the next transfer. HRDY goes into the high-impedance state when EMU1/$\overline{OFF}$ is low.
$\overline{HINT}$/TOUT1	O/Z	Interrupt. This output is used to interrupt the host. When the DSP is in reset, $\overline{HINT}$ is driven high. $\overline{HINT}$ can also be configured as the timer 1 output (TOUT1) when the HPI is disabled. The signal goes into the high-impedance state when EMU1/$\overline{OFF}$ is low.
HPIENA	I	HPI module select. HPIENA must be driven high during reset to enable the HPI. An internal pulldown resistor is always active and the HPIENA pin is sampled on the rising edge of $\overline{RS}$. If HPIENA is left open or is driven low during reset, the HPI module is disabled. Once the HPI is disabled, the HPIENA pin has no effect until the UC5402 is reset.
SUPPLY PINS		
CV_{DD}	S	$+V_{DD}$. Dedicated power supply for the core CPU
DV_{DD}	S	$+V_{DD}$. Dedicated power supply for the I/O pins
V_{SS}	S	Ground
MISCELLANEOUS SIGNAL		
NC		No connection
TEST PINS		
TCK	I	IEEE standard 1149.1 (JTAG) test clock. TCK is normally a free-running clock signal with a 50% duty cycle. The changes on the test access port (TAP) of input signals TMS and TDI are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK.
TDI	I	IEEE standard 1149.1 test data input pin with internal pullup device. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	O/Z	IEEE standard 1149.1 test data output. The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state except when the scanning of data is in progress. TDO also goes into the high-impedance state when EMU1/$\overline{OFF}$ is low.
TMS	I	IEEE standard 1149.1 test mode select. Pin with internal pullup device. This serial control input is clocked into the TAP controller on the rising edge of TCK.
$\overline{TRST}$	I	IEEE standard 1149.1 test reset. $\overline{TRST}$, when high, gives the IEEE standard 1149.1 scan system control of the operations of the device. If $\overline{TRST}$ is not connected or is driven low, the device operates in its functional mode, and the IEEE standard 1149.1 signals are ignored. Pin with internal pulldown device.
EMU0	I/O/Z	Emulator 0 pin. When $\overline{TRST}$ is driven low, EMU0 must be high for activation of the $\overline{OFF}$ condition. When $\overline{TRST}$ is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output by way of the IEEE standard 1149.1 scan system.
EMU1/$\overline{OFF}$	I/O/Z	Emulator 1 pin/disable all outputs. When $\overline{TRST}$ is driven high, EMU1/$\overline{OFF}$ is used as an interrupt to or from the emulator system and is defined as input/output by way of the IEEE standard 1149.1 scan system. When $\overline{TRST}$ is driven low, EMU1/$\overline{OFF}$ is configured as $\overline{OFF}$. The EMU1/$\overline{OFF}$ signal, when active (low), puts all output drivers into the high-impedance state. Note that $\overline{OFF}$ is used exclusively for testing and emulation purposes (not for multiprocessing applications). Therefore, for the $\overline{OFF}$ feature, the following apply: $\overline{TRST}$ = low EMU0 = high EMU1/$\overline{OFF}$ = low

† I = input, O = output, Z = high impedance, S = supply

‡ If an external clock source is used, the CLKIN signal level should not exceed CV_{DD} + 0.3 V.

2 Functional Overview

The following functional overview is based on the block diagram in Figure 2–1.

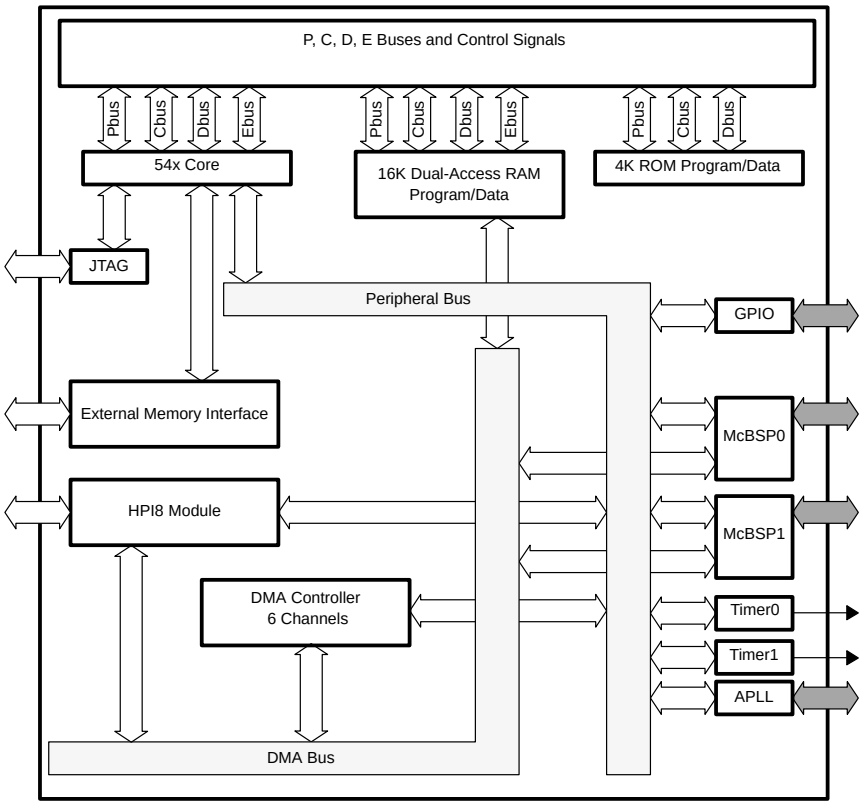


Figure 2–1. Block Diagram of the TMS320UC5402

2.1 Memory

The UC5402 device provides both on-chip ROM and RAM to aid in system performance and integration.

2.1.1 On-Chip Dual-Access RAM (DARAM)

The UC5402 device contains 16K × 16-bit of on-chip dual-access RAM (DARAM). The DARAM is composed of two blocks of 8K words each. Each block in the DARAM can support two reads in one cycle, or a read and a write in one cycle. The DARAM is located in the address range 0080h–3FFFh in data space, and can be mapped into program/data space by setting the OVLY bit to 1.

2.1.2 On-Chip ROM With Bootloader

The UC5402 features 4K × 16-bit of on-chip maskable ROM. Customers can arrange to have the ROM of the UC5402 programmed with contents unique to any particular application. A security option is available to protect a custom ROM. This security option is described in the *TMS320C54x DSP Reference Set, Volume 1: CPU and Peripherals* (literature number SPRU131). Note that only the ROM security option, and not the ROM/RAM option, is available on the UC5402 .

A bootloader is available in the standard UC5402 on-chip ROM. This bootloader can be used to automatically transfer user code from an external source to anywhere in the program memory at power up. If the MP/$\overline{MC}$ pin is sampled low during a hardware reset, execution begins at location FF80h of the on-chip ROM. This location contains a branch instruction to the start of the bootloader program. The standard UC5402 bootloader provides different ways to download the code to accomodate various system requirements:

- Parallel from 8-bit or 16-bit-wide EPROM
- Parallel from I/O space 8-bit or 16-bit mode
- Serial boot from serial ports 8-bit or 16-bit mode
- Host-port interface boot

The standard on-chip ROM layout is shown in Table 2–1.

Table 2–1. Standard On-Chip ROM Layout†

ADDRESS RANGE	DESCRIPTION
F000h – F7FFh	Reserved
F800h – FBFFh	Bootloader
FC00h – FCFFh	μ-law expansion table
FD00h – FDFFh	A-law expansion table
FE00h – FEFFh	Sine look-up table
FF00h – FF7Fh	Reserved
FF80h – FFFFh	Interrupt vector table

† In the UC5402 ROM, 128 words are reserved for factory device-testing purposes. Application code to be implemented in on-chip ROM must reserve these 128 words at addresses FF00h–FF7Fh in program space.

2.1.3 Memory Map

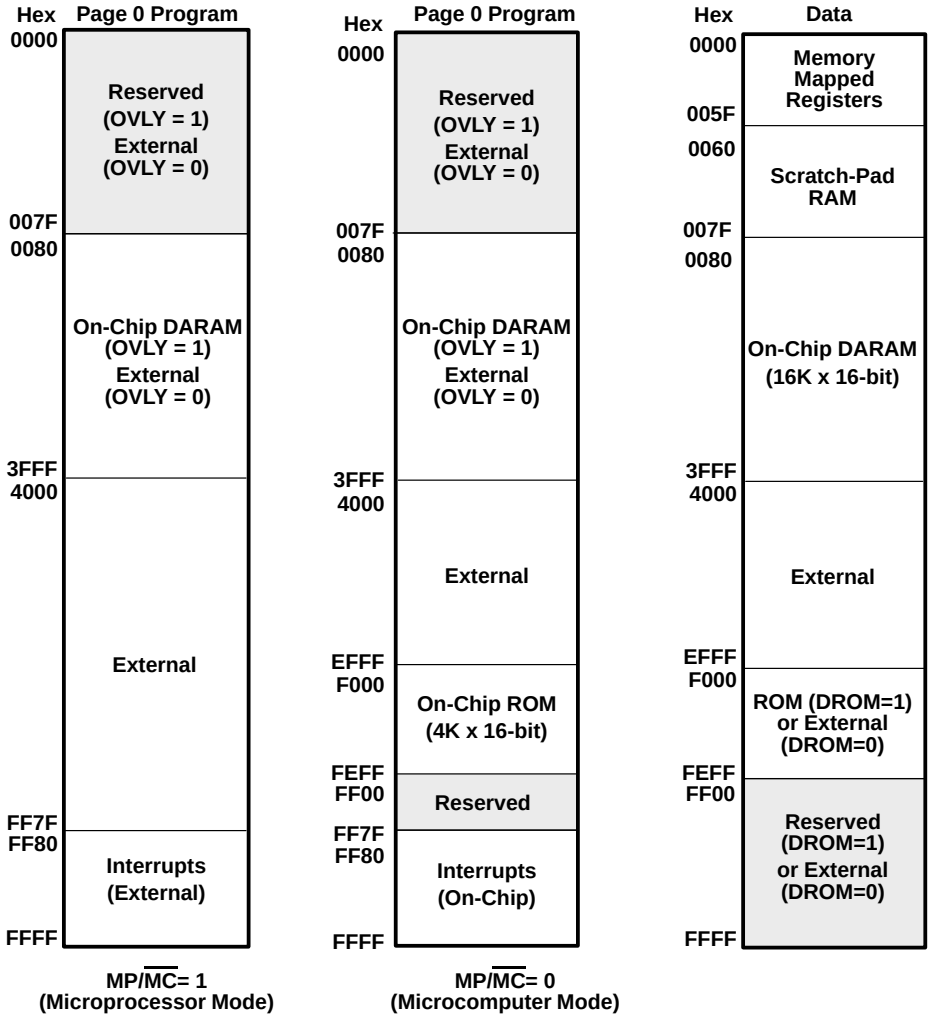


Figure 2–2. TMS320UC5402 Memory Map

2.1.4 Relocatable Interrupt Vector Table

The reset, interrupt, and trap vectors are addressed in program space. These vectors are soft — meaning that the processor, when taking the trap, loads the program counter (PC) with the trap address and executes the code at the vector location. Four words are reserved at each vector location to accommodate a delayed branch instruction, either two 1-word instructions or one 2-word instruction, which allows branching to the appropriate interrupt service routine with minimal overhead.

At device reset, the reset, interrupt, and trap vectors are mapped to address FF80h in program space. However, these vectors can be remapped to the beginning of any 128-word page in program space after device reset. This is done by loading the interrupt vector pointer (IPTR) bits in the PMST register (see Figure 2–3) with the appropriate 128-word page boundary address. After loading IPTR, any user interrupt or trap vector is mapped to the new 128-word page.

NOTE: The hardware reset ($\overline{RS}$) vector cannot be remapped because a hardware reset loads the IPTR with 1s. Therefore, the reset vector is always fetched at location FF80h in program space.

15 – 7	6	5	4	3	2	1	0
IPTR	MP/$\overline{MC}$	OVLY	AVIS	DROM	CLK OFF	SMUL	SST
R/W	R/W	R/W	R	R	R	R/W	R/W

LEGEND: R = Read, W = Write

Figure 2–3. Processor Mode Status (PMST) Register

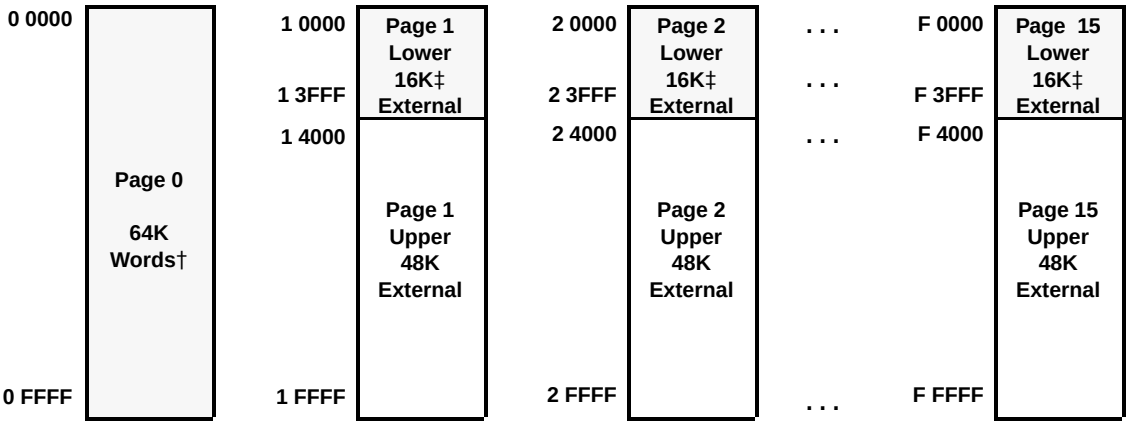
2.1.5 Extended Program Memory

The UC5402 uses a paged extended memory scheme in program space to allow access of up to 1024K program memory locations. In order to implement this scheme, the UC5402 includes several features that are also present on the 548/549 devices:

- Twenty address lines, instead of sixteen
- An extra memory-mapped register, the XPC register, defines the page selection. This register is memory-mapped into data space to address 001Eh. At a hardware reset, the XPC is initialized to 0.
- Six extra instructions for addressing extended program space. These six instructions affect the XPC.
  - *FB[D]* pmad (20 bits) – Far branch
  - *FBACC[D]* Accu[19:0] – Far branch to the location specified by the value in accumulator A or accumulator B
  - *FCALL[D]* pmad (20 bits) – Far call
  - *FCALA[D]* Accu[19:0] – Far call to the location specified by the value in accumulator A or accumulator B
  - *FRET[D]* – Far return
  - *FRETE[D]* – Far return with interrupts enabled
- In addition to these new instructions, two 54x instructions are extended to use 20 bits in the UC5402:
  - READA data_memory (using 20-bit accumulator address)
  - WRITA data_memory (using 20-bit accumulator address)

All other instructions, software interrupts, and hardware interrupts do not modify the XPC register and access only memory within the current page.

Program memory in the UC5402 is organized into 16 pages that are each 64K in length, as shown in Figure 2–4.



† See Figure 2–2

‡ The lower 16K words of pages 1 through 15 are available only when the OVLY bit is cleared to 0. If the OVLY bit is set to 1, the on-chip RAM is mapped to the lower 16K words of all program space pages.

Figure 2–4. Extended Program Memory

2.2 On-Chip Peripherals

The UC5402 device supports the following on-chip peripherals:

- Software-programmable wait-state generator with programmable bank-switching wait states
- An enhanced 8-bit host-port interface (HPI8)
- Two multichannel buffered serial ports (McBSPs)
- Two hardware timers
- A clock generator with a phase-locked loop (PLL)
- A direct memory access (DMA) controller

2.2.1 Software-Programmable Wait-State Generator

The software wait-state generator of the UC5402 can extend external bus cycles by up to fourteen machine cycles. Devices that require more than fourteen wait states can be interfaced using the hardware READY line. When all external accesses are configured for zero wait states, the internal clocks to the wait-state generator are automatically disabled. Disabling the wait-state generator clocks reduces the power consumption of the UC5402.

The software wait-state register (SWWSR) controls the operation of the wait-state generator. The 15 LSBs of the SWWSR specify the number of wait states (0 to 7) to be inserted for external memory accesses to five separate address ranges. This allows a different number of wait states for each of the five address ranges. Additionally, the software wait-state multiplier (SWSM) bit of the software wait-state control register (SWCR) defines a multiplication factor of 1 or 2 for the number of wait states. At reset, the wait-state generator is initialized to provide seven wait states on all external memory accesses. The SWWSR bit fields are shown in Figure 2–5 and described in Table 2–2.

15	14 – 12	11 – 9	8 – 6	5 – 3	2 – 0
XPA	I/O	Data	Data	Program	Program
R/W-0	R/W-111	R/W-111	R/W-111	R/W-111	R/W-111

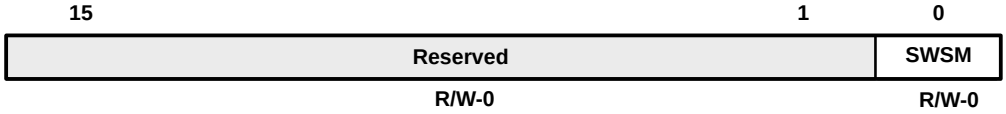
LEGEND: R=Read, W=Write, 0=Value after reset

Figure 2–5. Software Wait-State Register (SWWSR) [Memory-Mapped Register (MMR) Address 0028h]

Table 2–2. Software Wait-State Register (SWWSR) Bit Fields

BIT NO.	BIT NAME	RESET VALUE	FUNCTION
15	XPA	0	Extended program address control bit. XPA is used in conjunction with the program space fields (bits 0 through 5) to select the address range for the program space wait states.
14–12	I/O	1	I/O space. The field value (0–7) corresponds to the base number of wait states for I/O space accesses within addresses 0000–FFFFh. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.
11–9	Data	1	Upper data space. The field value (0–7) corresponds to the base number of wait states for external data space accesses within addresses 8000–FFFFh. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.
8–6	Data	1	Lower data space. The field value (0–7) corresponds to the base number of wait states for external data space accesses within addresses 0000–7FFFh. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.
5–3	Program	1	Upper program space. The field value (0–7) corresponds to the base number of wait states for external program space accesses within the following addresses: ❑ XPA = 0: x8000 – xFFFFh ❑ XPA = 1: The upper program space bit field has no effect on wait states. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.
2–0	Program	1	Program space. The field value (0–7) corresponds to the base number of wait states for external program space accesses within the following addresses: ❑ XPA = 0: x0000–x7FFFh ❑ XPA = 1: 00000–FFFFFh The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.

The software wait-state multiplier bit (SWSM) of the software wait-state control register (SWCR) is used to extend the base number of wait states selected by the SWWSR. The SWCR bit fields are shown in Figure 2–6 and described in Table 2–3.



LEGEND: R = Read, W = Write

Figure 2–6. Software Wait-State Control Register (SWCR) [MMR Address 002Bh]

Table 2–3. Software Wait-State Control Register (SWCR) Bit Fields

BIT NO.	BIT NAME	RESET VALUE	FUNCTION
15–1	Reserved	0	These bits are reserved and are unaffected by writes.
0	SWSM	0	Software wait-state multiplier. Used to multiply the number of wait states defined in the SWWSR by a factor of 1 or 2. ❑ SWSM = 0: wait-state base values are unchanged (multiplied by 1). ❑ SWSM = 1: wait-state base values are mulitplied by 2 for a maximum of 14 wait states.

2.2.1.1 Programmable Bank-Switching Wait States

The programmable bank-switching logic of the UC5402 is functionally equivalent to that of the 548/549 devices. This feature automatically inserts one cycle when accesses cross memory-bank boundaries within program or data memory space. A bank-switching wait state can also be automatically inserted when accesses cross the data space boundary into program space.

The bank-switching control register (BSCR) defines the bank size for bank-switching wait states. Figure 2–7 shows the BSCR and its bits are described in Table 2–4.

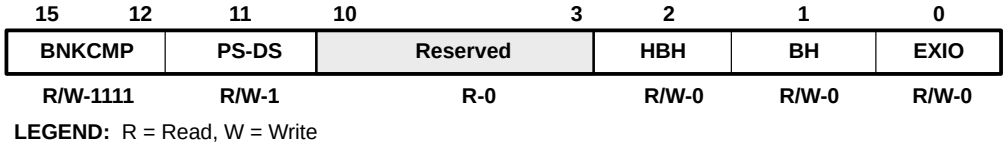


Figure 2–7. Bank-Switching Control Register (BSCR) [MMR Address 0029h]

Table 2–4. Bank-Switching Control Register (BSCR) Bit Fields

BIT NO.	BIT NAME	RESET VALUE	FUNCTION
15–12	BNKCMP	1111	Bank compare. Determines the external memory-bank size. BNKCMP is used to mask the four MSBs of an address. For example, if BNKCMP = 1111b, the four MSBs (bits 12–15) are compared, resulting in a bank size of 4K words. Bank sizes of 4K words to 64K words are allowed.
11	PS - DS	1	Program read – data read access. Inserts an extra cycle between consecutive accesses of program read and data read or data read and program read. PS-DS = 0 No extra cycles are inserted by this feature. PS-DS = 1 One extra cycle is inserted between consecutive data and program reads.
10–3	Reserved	0	These bits are reserved and are unaffected by writes.
2	HBH	0	HPI Bus holder. Controls the HPI bus holder feature. HBH is cleared to 0 at reset. HBH = 0 The bus holder is disabled. HBH = 1 The bus holder is enabled. When not driven, the HPI data bus (HD[7:0]) is held in the previous logic level.
1	BH	0	Bus holder. Controls the data bus holder feature. BH is cleared to 0 at reset. BH = 0 The bus holder is disabled. BH = 1 The bus holder is enabled. When not driven, the data bus (D[15:0]) is held in the previous logic level.
0	EXIO	0	External bus interface off. The EXIO bit controls the external bus-off function. EXIO = 0 The external bus interface functions as usual. EXIO = 1 The address bus, data bus, and control signals become inactive after completing the current bus cycle. Note that the DROM, MP/$\overline{MC}$, and OVLY bits in the PMST and the HM bit of ST1 cannot be modified when the interface is disabled.

2.2.2 Parallel I/O Ports

The UC5402 has a total of 64K I/O ports. These ports can be addressed by the PORTR instruction or the PORTW instruction. The $\overline{IS}$ signal indicates a read/write operation through an I/O port. The UC5402 can interface easily with external devices through the I/O ports while requiring minimal off-chip address-decoding circuits.

2.2.2.1 Enhanced 8-Bit Host-Port Interface (HPI8)

The UC5402 host-port interface, also referred to as the HPI8, is an enhanced version of the standard 8-bit HPI found on earlier 54x DSPs (542, 545, 548, and 549). The HPI8 is an 8-bit parallel port for interprocessor communication. The features of the HPI8 include:

Standard features:

- Sequential transfers (with autoincrement) or random-access transfers
- Host interrupt and 54x interrupt capability
- Multiple data strobes and control pins for interface flexibility

Enhanced features of the UC5402 HPI8:

- Access to entire on-chip RAM through DMA bus
- Capability to continue transferring during emulation stop

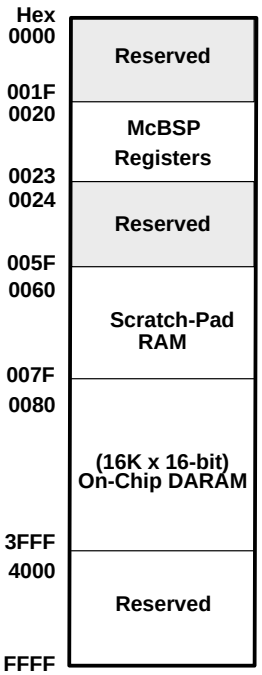


Figure 2–8. UC5402 HPI8 Memory Map

The HPI8 functions as a slave and enables the host processor to access the on-chip memory of the UC5402. A major enhancement to the UC5402 HPI over previous versions is that it allows host access to the entire on-chip memory range of the DSP. The host and the DSP both have access to the on-chip RAM at all times and host accesses are always synchronized to the DSP clock. If the host and the DSP contend for access to the same location, the host has priority, and the DSP waits for one HPI8 cycle. Note that since host accesses are always synchronized to the UC5402 clock, an active input clock (CLKIN) is required for HPI8 accesses during IDLE states, and host accesses are not allowed while the UC5402 reset pin is asserted.

The HPI8 interface consists of an 8-bit bidirectional data bus and various control signals. Sixteen-bit transfers are accomplished in two parts with the HBIL input designating high or low byte. The host communicates with the HPI8 through three dedicated registers — HPI address register (HPIA), HPI data register (HPID), and an HPI control register (HPIC). The HPIA and HPID registers are only accessible by the host, and the HPIC register is accessible by both the host and the UC5402.

2.2.2.2 Multichannel Buffered Serial Ports

The UC5402 device includes two high-speed, full-duplex multichannel buffered serial ports (McBSPs) that allow direct interface to other C54x/LC54x DSPs, codecs, and other devices in a system. The McBSPs are based on the standard serial port interface found on other 54x devices. Like its predecessors, the McBSP provides:

- Full-duplex communication
- Double-buffered data registers, which allow a continuous data stream
- Independent framing and clocking for receive and transmit

In addition, the McBSP has the following capabilities:

- Direct interface to:
  - T1/E1 framers
  - MVIP switching compatible and ST-BUS compliant devices
  - IOM-2 compliant devices
  - Serial peripheral interface devices
- Multichannel transmit and receive of up to 128 channels
- A wide selection of data sizes including 8, 12, 16, 20, 24, or 32 bits
- μ-law and A-law companding
- Programmable polarity for both frame synchronization and data clocks
- Programmable internal clock and frame generation

The McBSPs consist of separate transmit and receive channels that operate independently. The external interface of each McBSP consists of the following pins:

- BCLKX Transmit reference clock
- BDX Transmit data
- BFSX Transmit frame synchronization
- BCLKR Receive reference clock
- BDR Receive data
- BFSR Receive frame synchronization

The six pins listed are functionally equivalent to the previous serial port interface pins in the TMS320C5000™ platform of DSPs. On the transmitter, transmit frame synchronization and clocking are indicated by the BFSX and BCLKX pins, respectively. The CPU or DMA can initiate transmission of data by writing to the data transmit register (DXR). Data written to DXR is shifted out on the BDX pin through a transmit shift register (XSR). This structure allows DXR to be loaded with the next word to be sent while the transmission of the current word is in progress.

On the receiver, receive frame synchronization and clocking are indicated by the BFSR and BCLKR pins, respectively. The CPU or DMA can read received data from the data receive register (DRR). Data received on the BDR pin is shifted into a receive shift register (RSR) and then buffered in the receive buffer register (RBR). If the DRR is empty, the RBR contents are copied into the DRR. If not, the RBR holds the data until the DRR is available. This structure allows storage of the two previous words while the reception of the current word is in progress.

The CPU and DMA can move data to and from the McBSPs and can synchronize transfers based on McBSP interrupts, event signals, and status flags. The DMA is capable of handling data movement between the McBSPs and memory with no intervention from the CPU.

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In addition to the standard serial port functions, the McBSP provides programmable clock and frame synchronization generation. Among the programmable functions are:

- Frame synchronization pulse width
- Frame period
- Frame synchronization delay
- Clock reference (internal vs. external)
- Clock division
- Clock and frame synchronization polarity

The on-chip companding hardware allows compression and expansion of data in either μ-law or A-law format. When companding is used, transmit data is encoded according to specified companding law and received data is decoded to 2s complement format.

The McBSP allows multiple channels to be independently selected for the transmitter and receiver. When multiple channels are selected, each frame represents a time-division multiplexed (TDM) data stream. In using TDM data streams, the CPU may only need to process a few of them. Thus, to save memory and bus bandwidth, multichannel selection allows independent enabling of particular channels for transmission and reception. Up to 32 channels in a stream of up to 128 channels can be enabled.

The clock-stop mode (CLKSTP) in the McBSP provides compatibility with the serial peripheral interface (SPI) protocol. Clock-stop mode works with only single-phase frames and one word per frame. The word sizes supported by the McBSP are programmable for 8-, 12-, 16-, 20-, 24-, or 32-bit operation. When the McBSP is configured to operate in SPI mode, both the transmitter and the receiver operate together as a master or as a slave.

The McBSP is fully static and operates at arbitrarily low clock frequencies. The maximum frequency is CPU clock frequency divided by 2.

2.2.3 Hardware Timer

The UC5402 device features two 16-bit timing circuits with 4-bit prescalers. The main counter of each timer is decremented by one every CLKOUT cycle. Each time the counter decrements to 0, a timer interrupt is generated. The timers can be stopped, restarted, reset, or disabled by specific control bits.

2.2.4 Clock Generator

The clock generator provides clocks to the UC5402 device, and consists of an internal oscillator and a phase-locked loop (PLL) circuit. The clock generator requires a reference clock input, which can be provided by using a crystal resonator with the internal oscillator, or from an external reference clock source. The reference clock input is then divided by two or four (DIV mode) to generate clocks for the UC5402 device, or the PLL circuit can be used (PLL mode) to generate the device clock by multiplying the reference clock frequency by a scale factor. This allows the use of a clock source with a lower frequency than that of the CPU.The PLL is an adaptive circuit that, once synchronized, locks onto and tracks an input clock signal.

NOTE: If an external clock source is used, the CLKIN signal level should not exceed CV_{DD} + 0.3 V.

When the PLL is initially started, it enters a transitional mode during which the PLL acquires lock with the input signal. Once the PLL is locked, it continues to track and maintain synchronization with the input signal. Then, other internal clock circuitry allows the synthesis of new clock frequencies for use as master clock for the UC5402 device.

This clock generator allows system designers to select the clock source. The sources that drive the clock generator are:

- A crystal resonator circuit. The crystal resonator circuit is connected across the X1 and X2/CLKIN pins of the UC5402 to enable the internal oscillator.
- An external clock. The external clock source is directly connected to the X2/CLKIN pin, and X1 is left unconnected.

NOTE: If an external clock source is used, the CLKIN signal level should not exceed CV_{DD} + 0.3 V.

The software-programmable PLL features a high level of flexibility, and includes a clock scaler that provides various clock multiplier ratios, capability to directly enable and disable the PLL, and a PLL lock timer that can be used to delay switching to the PLL clocking mode of the device until lock is achieved. Devices that have a built-in software-programmable PLL can be configured in one of two clock modes:

- PLL mode. The input clock (X2/CLKIN) is multiplied by 1 of 31 possible ratios. These ratios are achieved using the PLL circuitry.
- DIV (divider) mode. The input clock is divided by 2 or 4. Note that when DIV mode is used, the PLL can be completely disabled to minimize power dissipation.

The software-programmable PLL is controlled using the 16-bit memory-mapped (address 0058h) clock mode register (CLKMD). The CLKMD register is used to define the clock configuration of the PLL clock module. Upon reset, the CLKMD register is initialized with a predetermined value dependent only upon the state of the CLKMD1 – CLKMD3 pins as shown in Table 2–5.

Table 2–5. Clock Mode Settings at Reset

CLKMD1	CLKMD2	CLKMD3	CLKMD RESET VALUE	CLOCK MODE
0	0	0	E007h	PLL x 15
0	0	1	9007h	PLL x 10
0	1	0	4007h	PLL x 5
1	0	0	1007h	PLL x 2
1	1	0	F007h	PLL x 1
1	1	1	0000h	1/2 (PLL disabled)
1	0	1	F000h	1/4 (PLL disabled)
0	1	1	—	Reserved (bypass mode)

2.2.5 DMA Controller

The UC5402 direct memory access (DMA) controller transfers data between points in the memory map without intervention by the CPU. The DMA controller allows movements of data to and from internal program/data memory or internal peripherals (such as the McBSPs) to occur in the background of CPU operation. The DMA has six independent programmable channels, allowing six different contexts for DMA operation.

2.2.5.1 Features

The DMA has the following features:

- The DMA operates independently of the CPU.
- The DMA has six channels. The DMA can keep track of the contexts of six independent block transfers.
- The DMA has higher priority than the CPU for internal accesses.
- Each channel has independently programmable priorities.
- Each channel's source and destination address registers can have configurable indexes through memory on each read and write transfer, respectively. The address may remain constant, be postincremented, postdecremented, or be adjusted by a programmable value.
- Each read or write transfer may be initialized by selected events.
- Upon completion of a half-block or an entire-block transfer, each DMA channel may send an interrupt to the CPU.
- The DMA can perform double-word transfers (a 32-bit transfer of two 16-bit words).

2.2.5.2 DMA Memory Map

The DMA memory map allows DMA transfers to be unaffected by the status of the MP/$\overline{\text{MC}}$, DROM, and OVLY bits. The DMA memory map (see Figure 2–9) is identical to that of the HPI8 controller .

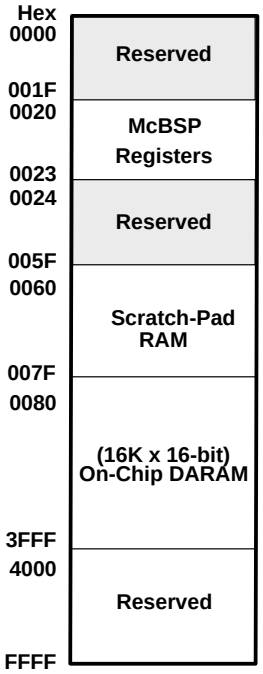

Figure 2–9. UC5402 DMA Memory Map

2.2.5.3 DMA Priority Level

Each DMA channel can be independently assigned high priority or low priority relative to each other. Multiple DMA channels that are assigned to the same priority level are handled in a round-robin manner.

2.2.5.4 DMA Source/Destination Address Modification

The DMA provides flexible address-indexing modes for easy implementation of data management schemes such as autobuffering and circular buffers. Source and destination addresses can be indexed separately and can be postincremented, postdecremented, or postincremented with a specified index offset.

2.2.5.5 DMA in Autoinitialization Mode

The DMA can automatically reinitialize itself after completion of a block transfer. Some of the DMA registers can be preloaded for the next block transfer through the DMA global reload registers (DMGSA, DMGDA, and DMGCR). Autoinitialization allows:

- Continuous operation: Normally, the CPU would have to reinitialize the DMA immediately after the completion of the current block transfer; but with the global reload registers, it can reinitialize these values for the next block transfer any time after the current block transfer begins.
- Repetitive operation: The CPU does not preload the global reload register with new values for each block transfer but only loads them on the first block transfer.

2.2.5.6 DMA Transfer Counting

The DMA channel element count register (DMCTRx) and the frame count register (DMFRCx) contain bit fields that represent the number of frames and the number of elements per frame to be transferred.

- Frame count. This 8-bit value defines the total number of frames in the block transfer. The maximum number of frames per block transfer is 128 (FRAME COUNT= 0ffh). The counter is decremented upon the last read transfer in a frame transfer. Once the last frame is transferred, the selected 8-bit counter is reloaded with the DMA global frame reload register (DMGFR) if the AUTOINIT bit is set to 1. A frame count of 0 (default value) means the block transfer contains a single frame.
- Element count. This 16-bit value defines the number of elements per frame. This counter is decremented after the read transfer of each element. The maximum number of elements per frame is 65536 (DMCTRn = 0FFFFh). In autoinitialization mode, once the last frame is transferred, the counter is reloaded with the DMA global count reload register (DMGCR).

2.2.5.7 DMA Transfers in Doubleword Mode

Doubleword mode allows the DMA to transfer 32-bit words in any index mode. In doubleword mode, two consecutive 16-bit transfers are initiated and the source and destination addresses are automatically updated following each transfer. In this mode, each 32-bit word is considered to be one element.

2.2.5.8 DMA Channel Index Registers

The particular DMA channel index register is selected by way of the SIND and DIND field in the DMA mode control register (DMMCRx). Unlike basic address adjustment, in conjunction with the frame index DMFRI0 and DMFRI1, the DMA allows different adjustment amounts depending on whether or not the element transfer is the last in the current frame. The normal adjustment value (element index) is contained in the element index registers DMIDX0 and DMIDX1. The adjustment value (frame index) for the end of the frame, is determined by the selected DMA frame index register, either DMFRI0 or DMFRI1.

The element index and the frame index affect address adjustment as follows:

- Element index: For all except the last transfer in the frame, the element index determines the amount to be added to the DMA channel for the source/destination address register (DMSRCx/DMDSTx) as selected by the SIND/DIND bits.
- Frame index: If the transfer is the last in a frame, the frame index is used for address adjustment as selected by the SIND/DIND bits. This occurs in both single-frame and multi-frame transfer.

2.2.5.9 DMA Interrupts

The ability of the DMA to interrupt the CPU based on the status of the data transfer is configurable and is determined by the IMOD and DINM bits in the DMA mode control register (DMMCRx). The available modes are shown in Table 2–6.

Table 2–6. DMA Interrupts

MODE	DINM	IMOD	INTERRUPT
ABU (non-decrement)	1	0	At full buffer only
ABU (non-decrement)	1	1	At half buffer and full buffer
Multi-Frame	1	0	At block transfer complete (DMCTRx = DMSEFCx[7:0] = 0)
Multi-Frame	1	1	At end of frame and end of block (DMCTRx = 0)
Either	0	X	No interrupt generated
Either	0	X	No interrupt generated

2.2.5.10 DMA Controller Synchronization Events

The transfers associated with each DMA channel can be synchronized to one of several events. The DSYN bit field of the DMA channel x sync select and frame count (DMSFCx) register selects the synchronization event for a channel. The list of possible events and the DSYN values are shown in Table 2–7.

Table 2–7. DMA Synchronization Events

DSYN VALUE	DMA SYNCHRONIZATION EVENT
0000b	No synchronization used
0001b	McBSP0 receive event
0010b	McBSP0 transmit event
0011–0100b	Reserved
0101b	McBSP1 receive event
0110b	McBSP1 transmit event
0111b–0110b	Reserved
1101b	Timer0 interrupt
1110b	External interrupt 3
1111b	Timer1 interrupt

2.2.5.11 DMA Channel Interrupt Selection

The DMA controller can generate a CPU interrupt for each of the six channels. However, the interrupt sources for channels 0,1, 2, and 3 are multiplexed with other interrupt sources. DMA channels 2 and 3 share an interrupt line with the receive and transmit portions of McBSP1 (IMR/IFR bits 10 and 11), and DMA channel 1 shares an interrupt line with timer 1 (IMR/IFR bit 7). The interrupt source for DMA channel 0 is shared with a reserved interrupt source. When the UC5402 is reset, the interrupts from these four DMA channels are deselected. The INTSEL bit field in the DMA channel priority and enable control (DMPREC) register can be used to select these interrupts, as shown in Table 2–8.

Table 2–8. DMA Channel Interrupt Selection

INTSEL Value	IMR/IFR[6]	IMR/IFR[7]	IMR/IFR[10]	IMR/IFR[11]
00b (reset)	Reserved	TINT1	BRINT1	BXINT1
01b	Reserved	TINT1	DMAC2	DMAC3
10b	DMAC0	DMAC1	DMAC2	DMAC3
11b	Reserved			

2.3 Memory-Mapped Registers

The UC5402 has a set of memory-mapped registers associated with the CPU, on-chip peripherals, the McBSPs, and the DMA.

2.3.1 CPU Memory-Mapped Registers

The UC5402 has 27 memory-mapped CPU registers, which are mapped in data memory space addresses 0h to 1Fh. Table 2–9 gives a list of the CPU memory-mapped registers (MMRs) available on UC5402.

Table 2–9. CPU Memory-Mapped Registers

NAME	ADDRESS		DESCRIPTION
	DEC	HEX	
IMR	0	0	Interrupt mask register
IFR	1	1	Interrupt flag register
–	2–5	2–5	Reserved for testing
ST0	6	6	Status register 0
ST1	7	7	Status register 1
AL	8	8	Accumulator A low word (15–0)
AH	9	9	Accumulator A high word (31–16)
AG	10	A	Accumulator A guard bits (39–32)
BL	11	B	Accumulator B low word (15–0)
BH	12	C	Accumulator B high word (31–16)
BG	13	D	Accumulator B guard bits (39–32)
TREG	14	E	Temporary register
TRN	15	F	Transition register
AR0	16	10	Auxiliary register 0
AR1	17	11	Auxiliary register 1
AR2	18	12	Auxiliary register 2
AR3	19	13	Auxiliary register 3
AR4	20	14	Auxiliary register 4
AR5	21	15	Auxiliary register 5
AR6	22	16	Auxiliary register 6
AR7	23	17	Auxiliary register 7
SP	24	18	Stack pointer register
BK	25	19	Circular buffer size register
BRC	26	1A	Block-repeat counter
RSA	27	1B	Block-repeat start address
REA	28	1C	Block-repeat end address
PMST	29	1D	Processor mode status (PMST) register
XPC	30	1E	Extended program page register
–	31	1F	Reserved

2.3.2 Peripheral Memory-Mapped Registers

The UC5402 has a set of memory-mapped registers associated with peripherals as shown in Table 2–10.

Table 2–10. Peripheral Memory-Mapped Registers

NAME	ADDRESS	DESCRIPTION	TYPE
DRR20	20h	McBSP0 data receive register 2	McBSP #0
DRR10	21h	McBSP0 data receive register 1	McBSP #0
DXR20	22h	McBSP0 data transmit register 2	McBSP #0
DXR10	23h	McBSP0 data transmit register 1	McBSP #0
TIM	24h	Timer0 register	Timer0
PRD	25h	Timer0 period counter	Timer0
TCR	26h	Timer0 control register	Timer0
–	27h	Reserved	
SWWSR	28h	Software wait-state register	External Bus
BSCR	29h	Bank-switching control register	External Bus
–	2Ah	Reserved	
SWCR	2Bh	Software wait-state control register	External Bus
HPIC	2Ch	HPI control register	HPI
–	2Dh–2Fh	Reserved	
TIM1	30h	Timer1 register	Timer1
PRD1	31h	Timer1 period counter	Timer1
TCR1	32h	Timer1 control register	Timer1
–	33h–37h	Reserved	
SPSA0	38h	McBSP0 subbank address register†	McBSP #0
SPSD0	39h	McBSP0 subbank data register†	McBSP #0
–	3Ah–3Bh	Reserved	
GPIOCR	3Ch	General-purpose I/O pins control register	GPIO
GPIOSR	3Dh	General-purpose I/O pins status register	GPIO
–	3Eh–3Fh	Reserved	
DRR21	40h	McBSP1 data receive register 2	McBSP #1
DRR11	41h	McBSP1 data receive register 1	McBSP #1
DXR21	42h	McBSP1 data transmit register 2	McBSP #1
DXR11	43h	McBSP1 data transmit register 1	McBSP #1
–	44h–47h	Reserved	
SPSA1	48h	McBSP1 subbank address register†	McBSP #1
SPSD1	49h	McBSP1 subbank data register†	McBSP #1
–	4Ah–53h	Reserved	
DMPREC	54h	DMA channel priority and enable control register	DMA
DMSA	55h	DMA subbank address register‡	DMA
DMSDI	56h	DMA subbank data register with autoincrement‡	DMA
DMSDN	57h	DMA subbank data register‡	DMA
CLKMD	58h	Clock mode register	PLL
–	59h–5Fh	Reserved	

† See Table 2–11 for a detailed description of the McBSP control registers and their subaddresses.
‡ See Table 2–12 for a detailed description of the DMA subbank addressed registers.

2.3.3 McBSP Control Registers and Subaddresses

The control registers for the multichannel buffered serial port (McBSP) are accessed using the subbank addressing scheme. This allows a set or subbank of registers to be accessed through a single memory location. The serial port subbank address (SPSA) register is used as a pointer to select a particular register within the subbank. The serial port subbank data (SPSD) register is used to access (read or write) the selected register. Table 2–11 shows the McBSP control registers and their corresponding subaddresses.

Table 2–11. McBSP Control Registers and Subaddresses

McBSP0		McBSP1		SUB-ADDRESS	DESCRIPTION
NAME	ADDRESS	NAME	ADDRESS		
SPCR10	39h	SPCR11	49h	00h	Serial port control register 1
SPCR20	39h	SPCR21	49h	01h	Serial port control register 2
RCR10	39h	RCR11	49h	02h	Receive control register 1
RCR20	39h	RCR21	49h	03h	Receive control register 2
XCR10	39h	XCR11	49h	04h	Transmit control register 1
XCR20	39h	XCR21	49h	05h	Transmit control register 2
SRGR10	39h	SRGR11	49h	06h	Sample rate generator register 1
SRGR20	39h	SRGR21	49h	07h	Sample rate generator register 2
MCR10	39h	MCR11	49h	08h	Multichannel register 1
MCR20	39h	MCR21	49h	09h	Multichannel register 2
RCERA0	39h	RCERA1	49h	0Ah	Receive channel enable register partition A
RCERB0	39h	RCERB1	49h	0Bh	Receive channel enable register partition B
XCERA0	39h	XCERA1	49h	0Ch	Transmit channel enable register partition A
XCERB0	39h	XCERB1	49h	0Dh	Transmit channel enable register partition B
PCR0	39h	PCR1	49h	0Eh	Pin control register

2.3.4 DMA Subbank Addressed Registers

The direct memory access (DMA) controller has several control registers associated with it. The main control register (DMPREC) is a standard memory-mapped register. However, the other registers are accessed using the subbank addressing scheme. This allows a set or subbank of registers to be accessed through a single memory location. The DMA subbank address (DMSA) register is used as a pointer to select a particular register within the subbank, while the DMA subbank data (DMSDN) register or the DMA subbank data register with autoincrement (DMSDI) is used to access (read or write) the selected register.

When the DMSDI register is used to access the subbank, the subbank address is automatically postincremented so that a subsequent access affects the next register within the subbank. This autoincrement feature is intended for efficient, successive accesses to several control registers. If the autoincrement feature is not required, the DMSDN register should be used to access the subbank. Table 2–12 shows the DMA controller subbank addressed registers and their corresponding subaddresses.

Table 2–12. DMA Subbank Addressed Registers

NAME	ADDRESS†	SUB-ADDRESS	DESCRIPTION
DMSRC0	56h/57h	00h	DMA channel 0 source address register
DMDST0	56h/57h	01h	DMA channel 0 destination address register
DMCTR0	56h/57h	02h	DMA channel 0 element count register
DMSFC0	56h/57h	03h	DMA channel 0 sync select and frame count register
DMMCR0	56h/57h	04h	DMA channel 0 transfer mode control register
DMSRC1	56h/57h	05h	DMA channel 1 source address register
DMDST1	56h/57h	06h	DMA channel 1 destination address register
DMCTR1	56h/57h	07h	DMA channel 1 element count register
DMSFC1	56h/57h	08h	DMA channel 1 sync select and frame count register
DMMCR1	56h/57h	09h	DMA channel 1 transfer mode control register
DMSRC2	56h/57h	0Ah	DMA channel 2 source address register
DMDST2	56h/57h	0Bh	DMA channel 2 destination address register
DMCTR2	56h/57h	0Ch	DMA channel 2 element count register
DMSFC2	56h/57h	0Dh	DMA channel 2 sync select and frame count register
DMMCR2	56h/57h	0Eh	DMA channel 2 transfer mode control register
DMSRC3	56h/57h	0Fh	DMA channel 3 source address register
DMDST3	56h/57h	10h	DMA channel 3 destination address register
DMCTR3	56h/57h	11h	DMA channel 3 element count register
DMSFC3	56h/57h	12h	DMA channel 3 sync select and frame count register
DMMCR3	56h/57h	13h	DMA channel 3 transfer mode control register
DMSRC4	56h/57h	14h	DMA channel 4 source address register
DMDST4	56h/57h	15h	DMA channel 4 destination address register
DMCTR4	56h/57h	16h	DMA channel 4 element count register
DMSFC4	56h/57h	17h	DMA channel 4 sync select and frame count register
DMMCR4	56h/57h	18h	DMA channel 4 transfer mode control register
DMSRC5	56h/57h	19h	DMA channel 5 source address register
DMDST5	56h/57h	1Ah	DMA channel 5 destination address register
DMCTR5	56h/57h	1Bh	DMA channel 5 element count register
DMSFC5	56h/57h	1Ch	DMA channel 5 sync select and frame count register
DMMCR5	56h/57h	1Dh	DMA channel 5 transfer mode control register
DMSRCP	56h/57h	1Eh	DMA source program page address (common channel)
DMDSTP	56h/57h	1Fh	DMA destination program page address (common channel)
DMIDX0	56h/57h	20h	DMA element index address register 0
DMIDX1	56h/57h	21h	DMA element index address register 1
DMFRI0	56h/57h	22h	DMA frame index register 0
DMFRI1	56h/57h	23h	DMA frame index register 1
DMGSA	56h/57h	24h	DMA global source address reload register
DMGDA	56h/57h	25h	DMA global destination address reload register
DMGCR	56h/57h	26h	DMA global count reload register
DMGFR	56h/57h	27h	DMA global frame count reload register

† Address 56h is used to access DMA subbank data registers with autoincrement (DMSDI) while address 57h is used to access DMA subbank data register without autoincrement (DMSDN).

2.4 Interrupts

Vector-relative locations and priorities for all internal and external interrupts are shown in Table 2–13.

Table 2–13. Interrupt Locations and Priorities

NAME	LOCATION DECIMAL	LOCATION HEX	PRIORITY	FUNCTION
$\overline{\text{RS}}$, SINTR	0	00	1	Reset (hardware and software reset)
$\overline{\text{NMI}}$, SINT16	4	04	2	Nonmaskable interrupt
SINT17	8	08	—	Software interrupt #17
SINT18	12	0C	—	Software interrupt #18
SINT19	16	10	—	Software interrupt #19
SINT20	20	14	—	Software interrupt #20
SINT21	24	18	—	Software interrupt #21
SINT22	28	1C	—	Software interrupt #22
SINT23	32	20	—	Software interrupt #23
SINT24	36	24	—	Software interrupt #24
SINT25	40	28	—	Software interrupt #25
SINT26	44	2C	—	Software interrupt #26
SINT27	48	30	—	Software interrupt #27
SINT28	52	34	—	Software interrupt #28
SINT29	56	38	—	Software interrupt #29
SINT30	60	3C	—	Software interrupt #30
$\overline{\text{INT0}}$, SINT0	64	40	3	External user interrupt #0
$\overline{\text{INT1}}$, SINT1	68	44	4	External user interrupt #1
$\overline{\text{INT2}}$, SINT2	72	48	5	External user interrupt #2
TINT0, SINT3	76	4C	6	Timer0 interrupt
BRINT0, SINT4	80	50	7	McBSP #0 receive interrupt
BXINT0, SINT5	84	54	8	McBSP #0 transmit interrupt
Reserved(DMAC0), SINT6	88	58	9	Reserved (default) or DMA channel 0 interrupt. The selection is made in the DMPREC register.
TINT1(DMAC1), SINT7	92	5C	10	Timer1 interrupt (default) or DMA channel 1 interrupt. The selection is made in the DMPREC register.
$\overline{\text{INT3}}$, SINT8	96	60	11	External user interrupt #3
HPINT, SINT9	100	64	12	HPI interrupt
BRINT1(DMAC2), SINT10	104	68	13	McBSP #1 receive interrupt (default) or DMA channel 2 interrupt. The selection is made in the DMPREC register.
BXINT1(DMAC3), SINT11	108	6C	14	McBSP #1 transmit interrupt (default) or DMA channel 3 interrupt. The selection is made in the DMPREC register.
DMAC4,SINT12	112	70	15	DMA channel 4 interrupt
DMAC5,SINT13	116	74	16	DMA channel 5 interrupt
Reserved	120–127	78–7F	—	Reserved

2.4.1 IFR and IMR Registers

The bits of the interrupt flag register (IFR) and interrupt mask register (IMR) are arranged as shown in Figure 2–10.

15–14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES	DMAC5	DMAC4	BXINT1 or DMAC3	BRINT1 or DMAC2	HPINT	INT3	TINT1 or DMAC1	RES or DMAC0	BXINT0	BRINT0	TINT0	INT2	INT1	INT0

Figure 2–10. IFR and IMR Registers

Table 2–14. IFR and IMR Register Bit Fields

BIT		FUNCTION
NUMBER	NAME	
15–14	–	Reserved for future expansion
13	DMAC5	DMA channel 5 interrupt flag/mask bit
12	DMAC4	DMA channel 4 interrupt flag/mask bit
11	BXINT1/DMAC3	This bit can be configured as either the McBSP1 transmit interrupt flag/mask bit, or the DMA channel 3 interrupt flag/mask bit. The selection is made in the DMPREC register.
10	BRINT1/DMAC2	This bit can be configured as either the McBSP1 receive interrupt flag/mask bit, or the DMA channel 2 interrupt flag/mask bit. The selection is made in the DMPREC register.
9	HPINT	Host to C54x interrupt flag/mask
8	INT3	External interrupt 3 flag/mask
7	TINT1/DMAC1	This bit can be configured as either the timer1 interrupt flag/mask bit, or the DMA channel 1 interrupt flag/mask bit. The selection is made in the DMPREC register.
6	Reserved or DMAC0	This bit can be configured either as reserved or as the DMA channel 0 interrupt flag/mask bit. The selection is made in the DMPREC register.
5	BXINT0	McBSP0 transmit interrupt flag/mask bit
4	BRINT0	McBSP0 receive interrupt flag/mask bit
3	TINT0	Timer 0 interrupt flag/mask bit
2	INT2	External interrupt 2 flag/mask bit
1	INT1	External interrupt 1 flag/mask bit
0	INT0	External interrupt 0 flag/mask bit

3 Documentation Support

Extensive documentation supports all TMS320™ DSP family of devices from product announcement through applications development. The following types of documentation are available to support the design and use of the C5000™ platform of DSPs:

- *TMS320C54x™ DSP Functional Overview* (literature number SPRU307)
- Device-specific data sheets
- Complete user's guides
- Development support tools
- Hardware and software application reports

The five-volume *TMS320C54x DSP Reference Set* (literature number SPRU210) consists of:

- *Volume 1: CPU and Peripherals* (literature number SPRU131)
- *Volume 2: Mnemonic Instruction Set* (literature number SPRU172)
- *Volume 3: Algebraic Instruction Set* (literature number SPRU179)
- *Volume 4: Applications Guide* (literature number SPRU173)
- *Volume 5: Enhanced Peripherals* (literature number SPRU302)

The reference set describes in detail the TMS320C54x™ DSP products currently available and the hardware and software applications, including algorithms, for fixed-point TMS320™ DSP family of devices.

A series of DSP textbooks is published by Prentice-Hall and John Wiley & Sons to support digital signal processing research and education. The TMS320™ DSP newsletter, *Details on Signal Processing*, is published quarterly and distributed to update TMS320™ DSP customers on product information.

Information regarding TI DSP products is also available on the Worldwide Web at *http://www.ti.com* uniform resource locator (URL).

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4 Electrical Specifications

This section provides the absolute maximum ratings and the recommended operating conditions for the TMS320UC5402 DSP.

4.1 Absolute Maximum Ratings

The list of absolute maximum ratings are specified over operating case temperature. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 4.2 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to V_{SS}. Figure 4–1 provides the test load circuit values for a 1.8-V device.

Supply voltage I/O range, DV_{DD} . . . . . –0.3 V to 4.0 V
Supply voltage core range, CV_{DD} . . . . . –0.3 V to 2.0 V
Input voltage range, V_I . . . . . –0.3 V to 4.5 V
Output voltage range, V_O . . . . . –0.3 V to 4.5 V
Operating case temperature range, T_C . . . . . –40°C to 100°C
Storage temperature range, T_{stg} . . . . . –55°C to 150°C

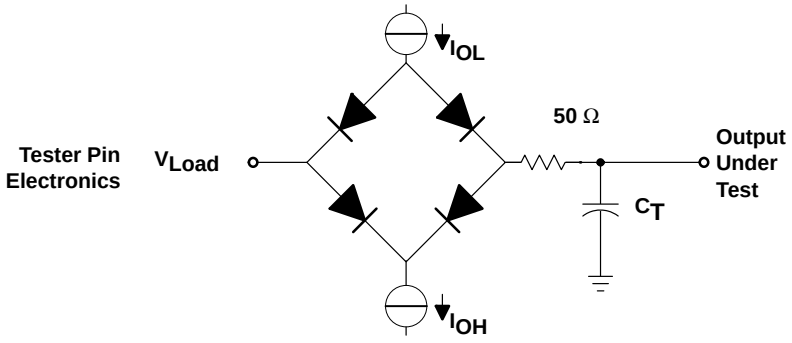
4.2 Recommended Operating Conditions

				MIN	NOM	MAX	UNIT
DV_{DD}	Device supply voltage, I/O			1.71		3.6	V
CV_{DD}	Device supply voltage, core			1.71	1.8	1.98	V
V_{SS}	Supply voltage, GND				0		V
V_{IH}	High-level input voltage	DV_{DD} = 1.71 V to 1.89 V	X2/CLKIN	1.35		CV_{DD} + 0.3	V
			All other inputs	1.35		DV_{DD} + 0.3	
		DV_{DD} = 1.90 V to 2.99 V	X2/CLKIN	1.35		CV_{DD} + 0.3	
			All other inputs	1.7		DV_{DD} + 0.3	
		DV_{DD} = 3.0 V to 3.6 V	X2/CLKIN	1.35		CV_{DD} + 0.3	
			$\overline{RS}$, $\overline{INTn}$, $\overline{NMI}$, $\overline{BIO}$, BCLKR0, BCLKR1, BCLKX0, BCLKX1, $\overline{HCS}$, $\overline{HDS1}$, $\overline{HDS2}$, TDI, TMS, CLKMDn	2.2		DV_{DD} + 0.3	
			TCK, $\overline{TRST}$	2.5		DV_{DD} + 0.3	
			All other inputs	2		DV_{DD} + 0.3	
V_{IL}	Low-level input voltage	DV_{DD} = 1.71 V to 1.89 V	X2/CLKIN	–0.3		0.6	V
			All other inputs	–0.3		0.6	
		DV_{DD} = 1.90 V to 3.6 V	X2/CLKIN	–0.3		0.6	
			$\overline{RS}$, $\overline{INTn}$, $\overline{NMI}$, $\overline{BIO}$, BCLKR0, BCLKR1, BCLKX0, BCLKX1, $\overline{HCS}$, $\overline{HDS1}$, $\overline{HDS2}$, TCK, CLKMDn	–0.3		0.6	
			All other inputs	–0.3		0.8	
I_{OH}	High-level output current					–300	µA
I_{OL}	Low-level output current					1.5	mA
T_C	Operating case temperature			–40		100	°C

4.3 Electrical Characteristics Over Recommended Operating Case Temperature Range (Unless Otherwise Noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = MAX		DV_{DD} – 0.3			V
V_{OL}	Low-level output voltage	DV_{DD} = 1.71 to 1.89 V	I_{OL} = MAX	CLKOUT			0.4	V
				All other outputs			0.35	
		DV_{DD} = 1.9 to 3.6 V	I_{OL} = MAX	All outputs			0.4	
I_{IZ}	Input current for outputs in high impedance	D[15:0], HD[7:0]	Bus holders enabled, DV_{DD} = MAX, $V_I = V_{SS}$ to DV_{DD}		–175		175	µA
		All other inputs	DV_{DD} = MAX, $V_O = V_{SS}$ to DV_{DD}		–5		5	
I_I	Input current	X2/CLKIN		($V_I = V_{SS}$ to DV_{DD})	–40		40	µA
		$\overline{TRST}$	With internal pulldown		–5		300	
		HPIENA	With internal pulldown		–5		300	
		TMS, TCK, TDI, HPI‡	With internal pullups, HPIENA = 0		–300		5	
		All other input-only pins			–5		5	
I_{DDC}	Supply current, core CPU		CV_{DD} = 1.8 V, f_{clock} = 80 MHz,§ T_C = 25°C			35		mA
I_{DDP}	Supply current, pins		f_{clock} = 80 MHz,§ T_C = 25°C	DV_{DD} = 1.71 to 1.89 V		12		mA
				DV_{DD} = 1.9 to 3.6 V		27		
I_{DD}	Supply current, standby	IDLE2	PLL × 1 mode, 80 MHz input			1.6		mA
		IDLE3	Divide-by-two mode, CLKIN stopped			20		µA
C_i	Input capacitance					5		pF
C_o	Output capacitance					5		pF

† All values are typical unless otherwise specified.
‡ HPI input signals except for HPIENA.
§ Clock mode: PLL × 1 with external source



Where: I_{OL} = 1.5 mA (all outputs)
I_{OH} = 300 µA (all outputs)
V_{Load} = 0.855 V
C_T = 40 pF typical load circuit capacitance

Figure 4–1. 1.8-V Test Load Circuit

4.4 Package Thermal Resistance Characteristics

Table 4–1 provides the estimated thermal resistance characteristics for the recommended package types used on the TMS320UC5402 DSP.

Table 4–1. Thermal Resistance Characteristics

PARAMETER	GGU PACKAGE	PGE PACKAGE	UNIT
$R_{\Theta JA}$	38	56	°C/W
$R_{\Theta JC}$	5	5	°C/W

4.5 Timing Parameter Symbology

Timing parameter symbols used in the timing requirements and switching characteristics tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

Lowercase subscripts and their meanings:

a	access time
c	cycle time (period)
d	delay time
dis	disable time
en	enable time
f	fall time
h	hold time
r	rise time
su	setup time
t	transition time
v	valid time
w	pulse duration (width)
X	Unknown, changing, or don’t care level

Letters and symbols and their meanings:

H	High
L	Low
V	Valid
Z	High impedance

4.6 Clock Options

The frequency of the reference clock provided at the CLKIN pin can be divided by a factor of two or four or multiplied by one of several values to generate the internal machine cycle.

4.6.1 Internal Oscillator With External Crystal

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN. The frequency of CLKOUT is a multiple of the oscillator frequency. The multiply ratio is determined by the bit settings in the CLKMD register. The crystal should be in fundamental-mode operation, and parallel resonant, with an effective series resistance of 30 Ω and power dissipation of 1 mW. The circuit shown in Figure 4–2 represents fundamental-mode operation.

The connection of the required circuit, consisting of the crystal and two load capacitors, is shown in Figure 4–2. The load capacitors, C_1 and C_2, should be chosen such that the equation below is satisfied. C_L in the equation is the load specified for the crystal.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

		MIN	MAX	UNIT
f_{clock}	Input clock frequency	10	20	MHz

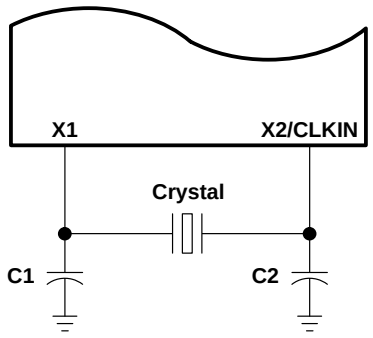


Figure 4–2. Internal Oscillator With External Crystal

4.6.2 Divide-By-Two Clock Option (PLL disabled)

The frequency of the reference clock provided at the X2/CLKIN pin can be divided by a factor of two to generate the internal machine cycle. The selection of the clock mode is described in the clock generator section.

When an external clock source is used, the external frequency injected must conform to specifications listed in Table 4–2.

NOTE: If an external clock source is used, the CLKIN signal level should not exceed CV_{DD} + 0.3 V.

Table 4–2 and Table 4–3 assume testing over recommended operating conditions and H = 0.5$t_{c(CO)}$ (see Figure 4–3).

Table 4–2. Divide-By-2 and Divide-by-4 Clock Options Timing Requirements

		MIN	MAX	UNIT
$t_{c(CI)}$	Cycle time, X2/CLKIN	6.25	†	ns
$t_{f(CI)}$	Fall time, X2/CLKIN		8	ns
$t_{r(CI)}$	Rise time, X2/CLKIN		8	ns

† This device utilizes a fully static design and therefore can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz.

Table 4–3. Divide-By-2 and Divide-by-4 Clock Options Switching Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$t_{c(CO)}$	Cycle time, CLKOUT	12.5‡	$2t_{c(CI)}$	†	ns
$t_{d(CIH-CO)}$	Delay time, X2/CLKIN high to CLKOUT high/low	7	12	20	ns
$t_{f(CO)}$	Fall time, CLKOUT		4		ns
$t_{r(CO)}$	Rise time, CLKOUT		4		ns
$t_{w(COL)}$	Pulse duration, CLKOUT low	H–2		H + 2	ns
$t_{w(COH)}$	Pulse duration, CLKOUT high	H–2		H + 2	ns

† This device utilizes a fully static design and therefore can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz.

‡ It is recommended that the PLL clocking option be used for maximum frequency operation.

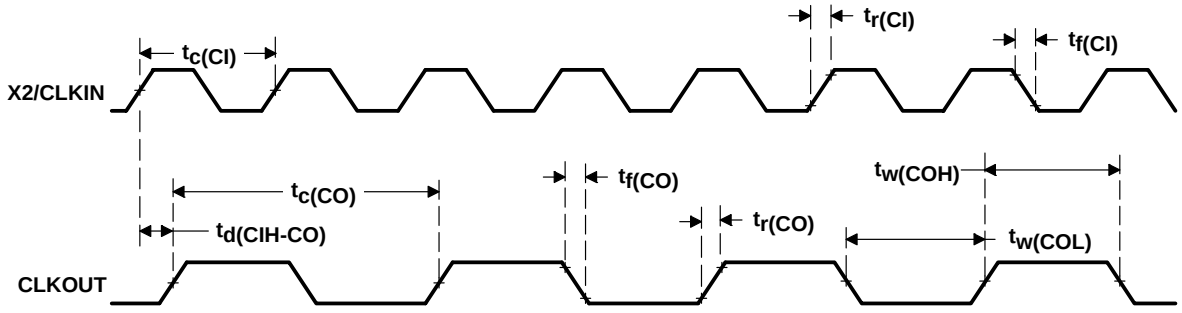


Figure 4–3. External Divide-by-Two Clock Timing

4.6.3 Multiply-By-N Clock Option (PLL Enabled)

The frequency of the reference clock provided at the X2/CLKIN pin can be multiplied by a factor of N to generate the internal machine cycle. The selection of the clock mode and the value of N is described in the clock generator section.

When an external clock source is used, the external frequency injected must conform to specifications listed in Table 4–4.

NOTE: If an external clock source is used, the CLKIN signal level should not exceed CV_{DD} + 0.3 V.

Table 4–4 and Table 4–5 assume testing over recommended operating conditions and H = 0.5$t_{c(CO)}$ (see Figure 4–4).

Table 4–4. Multiply-By-N Clock Option Timing Requirements†

			MIN	MAX	UNIT
$t_{c(CI)}$	Cycle time, X2/CLKIN	Integer PLL multiplier N (N = 1–15)	12.5N	400N	ns
		PLL multiplier N = x.5	12.5N	200N	
		PLL multiplier N = x.25, x.75	12.5N	100N	
$t_{f(CI)}$	Fall time, X2/CLKIN			8	ns
$t_{r(CI)}$	Rise time, X2/CLKIN			8	ns

† N = Multiplication factor

Table 4–5. Multiply-By-N Clock Option Switching Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$t_{c(CO)}$	Cycle time, CLKOUT	12.5	$t_{c(CI)}/N$†		ns
$t_{d(CI-CO)}$	Delay time, X2/CLKIN high/low to CLKOUT high/low	7	10	20	ns
$t_{f(CO)}$	Fall time, CLKOUT		4		ns
$t_{r(CO)}$	Rise time, CLKOUT		4		ns
$t_{w(COL)}$	Pulse duration, CLKOUT low	H–2		H + 2	ns
$t_{w(COH)}$	Pulse duration, CLKOUT high	H–2		H + 2	ns
t_p	Transitory phase, PLL lock up time			30	μs

† N = Multiplication factor

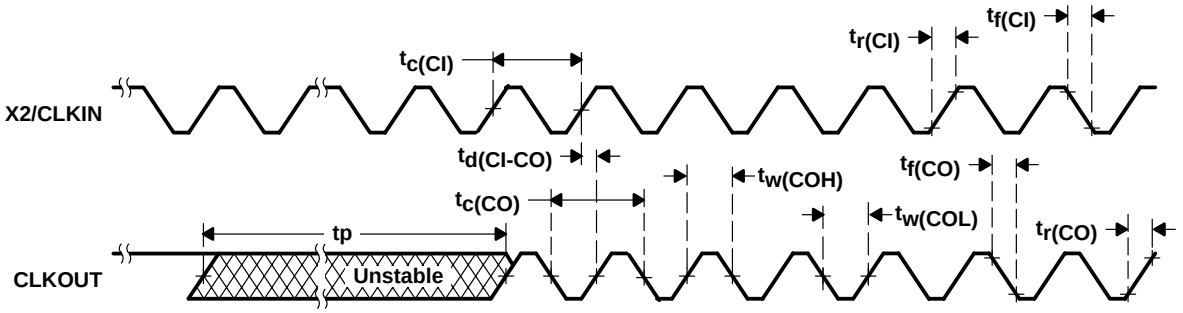


Figure 4–4. External Multiply-by-One Clock Timing

4.7 Memory and Parallel I/O Interface Timing

4.7.1 Memory Read

Table 4–6 and Table 4–7 assume testing over recommended operating conditions with $\overline{\text{MSTRB}}$ = 0 and H = 0.5$t_{c(CO)}$ (see Figure 4–5).

Table 4–6. Memory Read Timing Requirements†

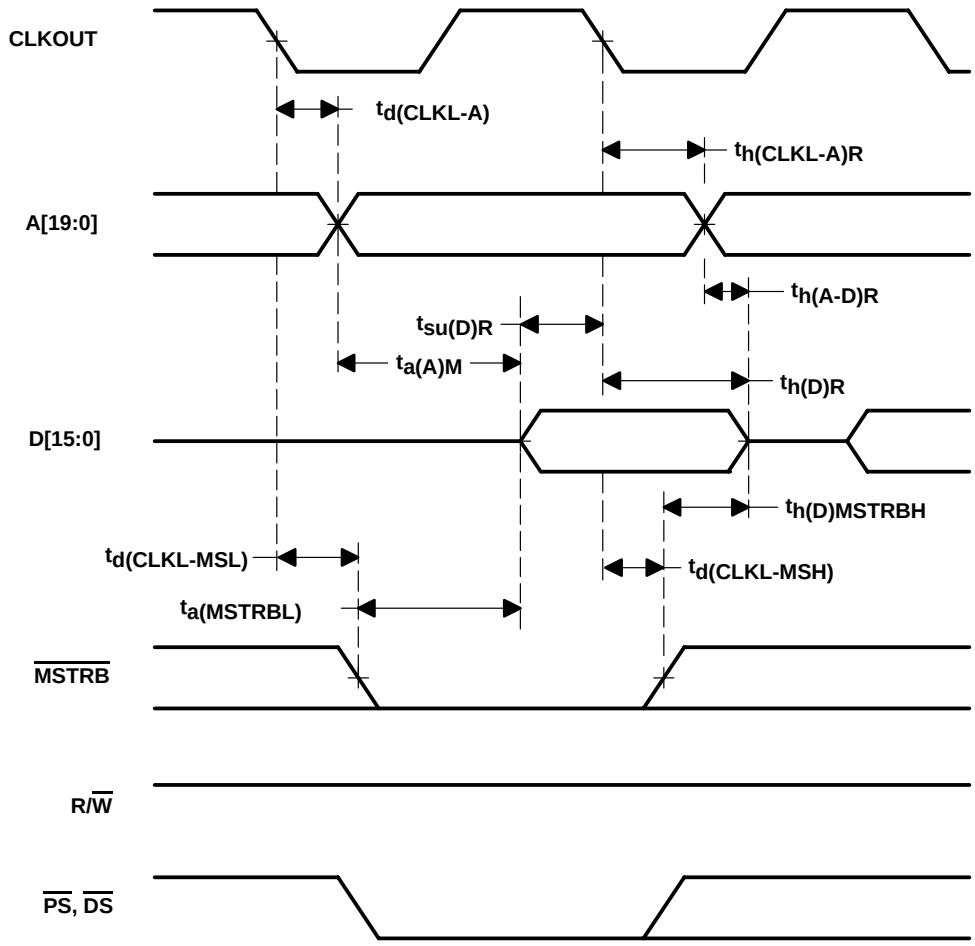
		MIN	MAX	UNIT
$t_{a(A)M}$	Access time, read data access from address valid		2H–14	ns
$t_{a(MSTRBL)}$	Access time, read data access from $\overline{\text{MSTRB}}$ low		2H–14	ns
$t_{su(D)R}$	Setup time, read data before CLKOUT low	7		ns
$t_{h(D)R}$	Hold time, read data after CLKOUT low	–2		ns
$t_{h(A-D)R}$	Hold time, read data after address invalid	–3		ns
$t_{h(D)MSTRBH}$	Hold time, read data after $\overline{\text{MSTRB}}$ high	–3		ns

† Address, $\overline{\text{PS}}$, and $\overline{\text{DS}}$ timings are all included in timings referenced as address.

Table 4–7. Memory Read Switching Characteristics†

PARAMETER		MIN	MAX	UNIT
$t_{d(CLKL-A)}$	Delay time, CLKOUT low to address valid‡	0	8	ns
$t_{d(CLKL-MSL)}$	Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ low	0	8	ns
$t_{d(CLKL-MSH)}$	Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ high	0	8	ns
$t_{h(CLKL-A)R}$	Hold time, address valid after CLKOUT low‡	0	7	ns
$t_{h(CLKH-A)R}$	Hold time, address valid after CLKOUT high§	0	5	ns

† Address, $\overline{\text{PS}}$, and $\overline{\text{DS}}$ timings are all included in timings referenced as address.
‡ In the case of a memory read preceded by a memory read
§ In the case of a memory read preceded by a memory write



NOTE A: A[19:16] are always driven low during external data space accesses.

Figure 4–5. Memory Read ($\overline{\text{MSTRB}}$ = 0)

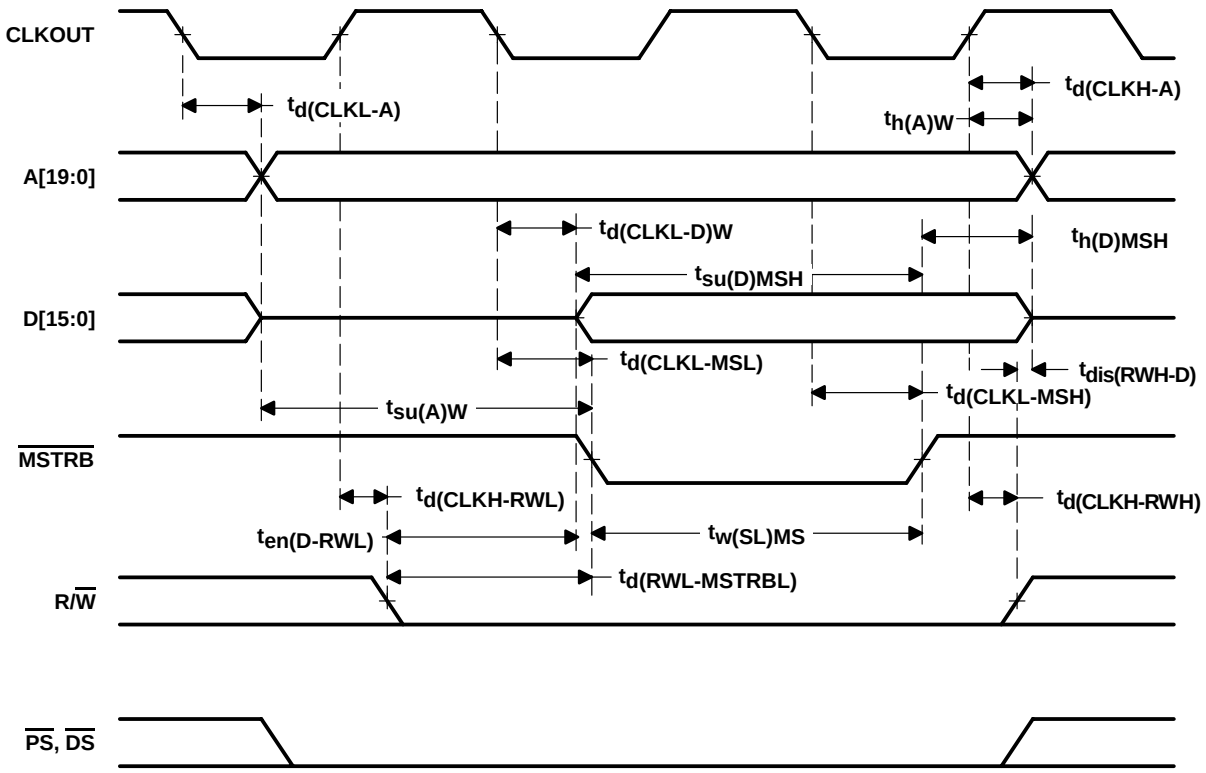
4.7.2 Memory Write

Table 4–8 assumes testing over recommended operating conditions with $\overline{\text{MSTRB}}$ = 0 and H = 0.5$t_{c(CO)}$ (see Figure 4–6).

Table 4–8. Memory Write Switching Characteristics†

PARAMETER		MIN	MAX	UNIT
$t_{d(CLKH-A)}$	Delay time, CLKOUT high to address valid‡	0	5	ns
$t_{d(CLKL-A)}$	Delay time, CLKOUT low to address valid§	0	8	ns
$t_{d(CLKL-MSL)}$	Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ low	0	8	ns
$t_{d(CLKL-D)W}$	Delay time, CLKOUT low to data valid	0	17	ns
$t_{d(CLKL-MSH)}$	Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ high	0	8	ns
$t_{d(CLKH-RWL)}$	Delay time, CLKOUT high to R/$\overline{\text{W}}$ low	–1	5	ns
$t_{d(CLKH-RWH)}$	Delay time, CLKOUT high to R/$\overline{\text{W}}$ high	–2	5	ns
$t_{d(RWL-MSTRBL)}$	Delay time, R/$\overline{\text{W}}$ low to $\overline{\text{MSTRB}}$ low	H – 4	H + 2	ns
$t_{h(A)W}$	Hold time, address valid after CLKOUT high‡	0	5	ns
$t_{h(D)MSH}$	Hold time, write data valid after $\overline{\text{MSTRB}}$ high	H–3	H+14	ns
$t_{w(SL)MS}$	Pulse duration, $\overline{\text{MSTRB}}$ low	2H–5		ns
$t_{su(A)W}$	Setup time, address valid before $\overline{\text{MSTRB}}$ low	2H–4		ns
$t_{su(D)MSH}$	Setup time, write data valid before $\overline{\text{MSTRB}}$ high	2H–14	2H+5	ns
$t_{en(D–RWL)}$	Enable time, data bus driven after R/$\overline{\text{W}}$ low	H–5		ns
$t_{dis(RWH–D)}$	Disable time, R/$\overline{\text{W}}$ high to data bus high impedance		0	ns

† Address, $\overline{\text{PS}}$, and $\overline{\text{DS}}$ timings are all included in timings referenced as address.
‡ In the case of a memory write preceded by a memory write
§ In the case of a memory write preceded by an I/O cycle



NOTE A: A[19:16] are always driven low during external data space accesses.

Figure 4–6. Memory Write ($\overline{\text{MSTRB}}$ = 0)

4.7.3 I/O Read

Table 4–9 and Table 4–10 assume testing over recommended operating conditions, $\overline{\text{IOSTRB}}$ = 0, and H = 0.5$t_{c(CO)}$ (see Figure 4–7).

Table 4–9. I/O Read Timing Requirements

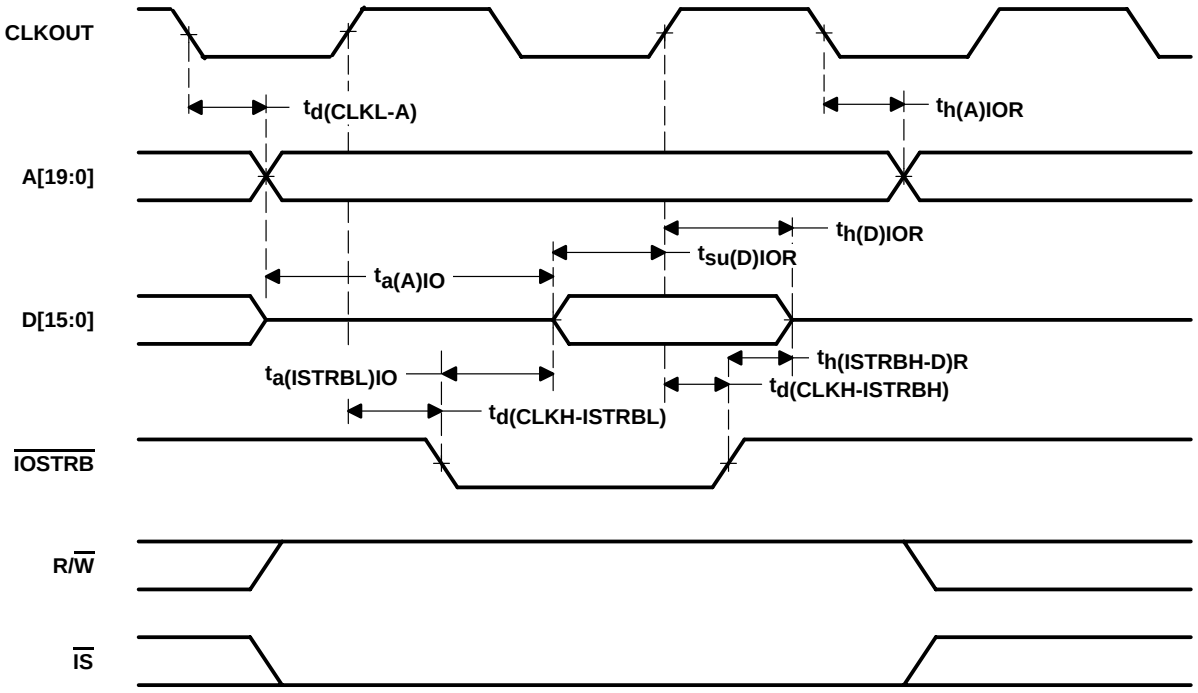
		MIN	MAX	UNIT
$t_{a(A)IO}$	Access time, read data access from address valid†		3H–17	ns
$t_{a(ISTRBL)IO}$	Access time, read data access from $\overline{\text{IOSTRB}}$ low		3H–17	ns
$t_{su(D)IOR}$	Setup time, read data before CLKOUT high	9		ns
$t_{h(D)IOR}$	Hold time, read data after CLKOUT high	–1		ns
$t_{h(ISTRBH-D)R}$	Hold time, read data after $\overline{\text{IOSTRB}}$ high	–3		ns

† Address and $\overline{\text{IS}}$ timings are included in timings referenced as address.

Table 4–10. I/O Read Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{d(CLKL-A)}$	Delay time, CLKOUT low to address valid†	0	8	ns
$t_{d(CLKH-ISTRBL)}$	Delay time, CLKOUT high to $\overline{\text{IOSTRB}}$ low	–2	5	ns
$t_{d(CLKH-ISTRBH)}$	Delay time, CLKOUT high to $\overline{\text{IOSTRB}}$ high	–2	5	ns
$t_{h(A)IOR}$	Hold time, address after CLKOUT low†	0	8	ns

† Address and $\overline{\text{IS}}$ timings are included in timings referenced as address.



NOTE A: A[19:16] are always driven low during I/O accesses.

Figure 4–7. Parallel I/O Port Read ($\overline{\text{IOSTRB}}$ = 0)

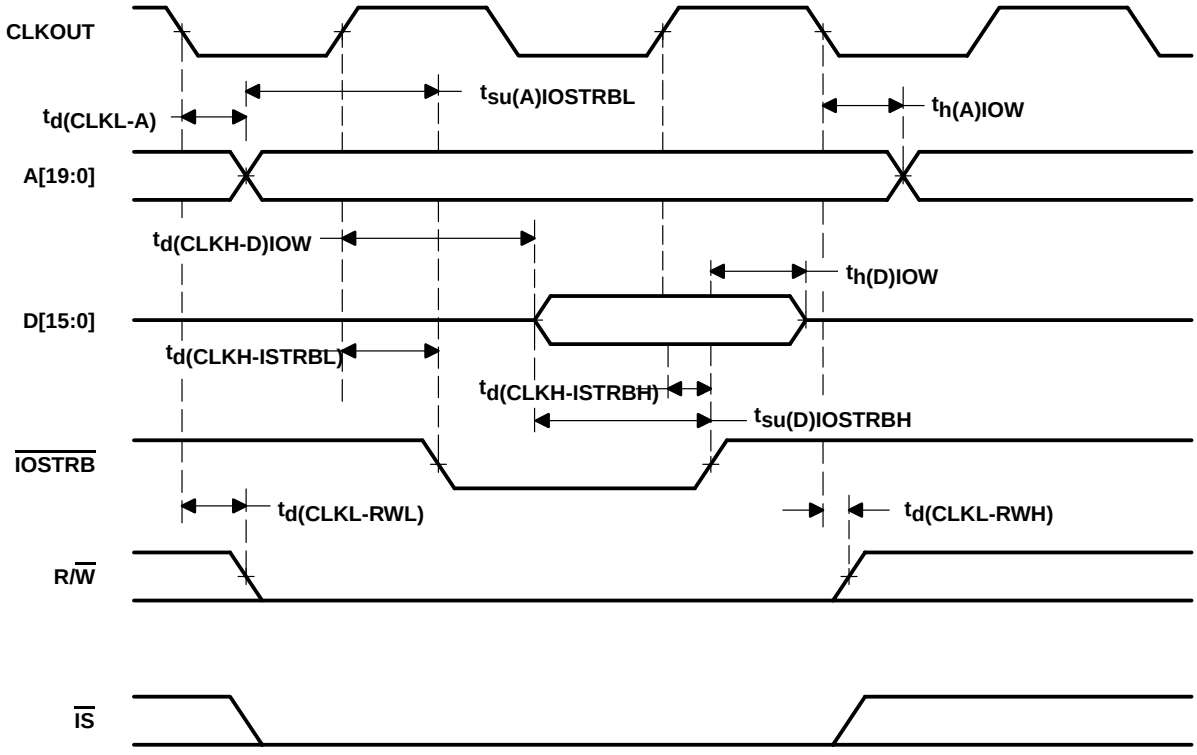
4.7.4 I/O Write

Table 4–11 assumes testing over recommended operating conditions, $\overline{\text{IOSTRB}}$ = 0, and H = 0.5$t_{c(CO)}$ (see Figure 4–8).

Table 4–11. I/O Write Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{d(CLKL-A)}$	Delay time, CLKOUT low to address valid†	0	8	ns
$t_{d(CLKH-ISTRBL)}$	Delay time, CLKOUT high to $\overline{\text{IOSTRB}}$ low	–2	5	ns
$t_{d(CLKH-D)IOW}$	Delay time, CLKOUT high to write data valid	H–5	H+14	ns
$t_{d(CLKH-ISTRBH)}$	Delay time, CLKOUT high to $\overline{\text{IOSTRB}}$ high	–2	5	ns
$t_{d(CLKL-RWL)}$	Delay time, CLKOUT low to R/$\overline{\text{W}}$ low	0	8	ns
$t_{d(CLKL-RWH)}$	Delay time, CLKOUT low to R/$\overline{\text{W}}$ high	0	8	ns
$t_{h(A)IOW}$	Hold time, address valid after CLKOUT low†	0	8	ns
$t_{h(D)IOW}$	Hold time, write data after $\overline{\text{IOSTRB}}$ high	H–3	H+11	ns
$t_{su(D)IOSTRBH}$	Setup time, write data before $\overline{\text{IOSTRB}}$ high	H–11	H+1	ns
$t_{su(A)IOSTRBL}$	Setup time, address valid before $\overline{\text{IOSTRB}}$ low†	H–2	H+2	ns

† Address and $\overline{\text{IS}}$ timings are included in timings referenced as address.



NOTE A: A[19:16] are always driven low during I/O accesses.

Figure 4–8. Parallel I/O Port Write ($\overline{\text{IOSTRB}}$ = 0)

4.8 Ready Timing for Externally Generated Wait States

Table 4–12 and Table 4–13 assume testing over recommended operating conditions and H = 0.5$t_{c(CO)}$ (see Figure 4–9 through Figure 4–12).

Table 4–12. Ready Timing Requirements for Externally Generated Wait States†

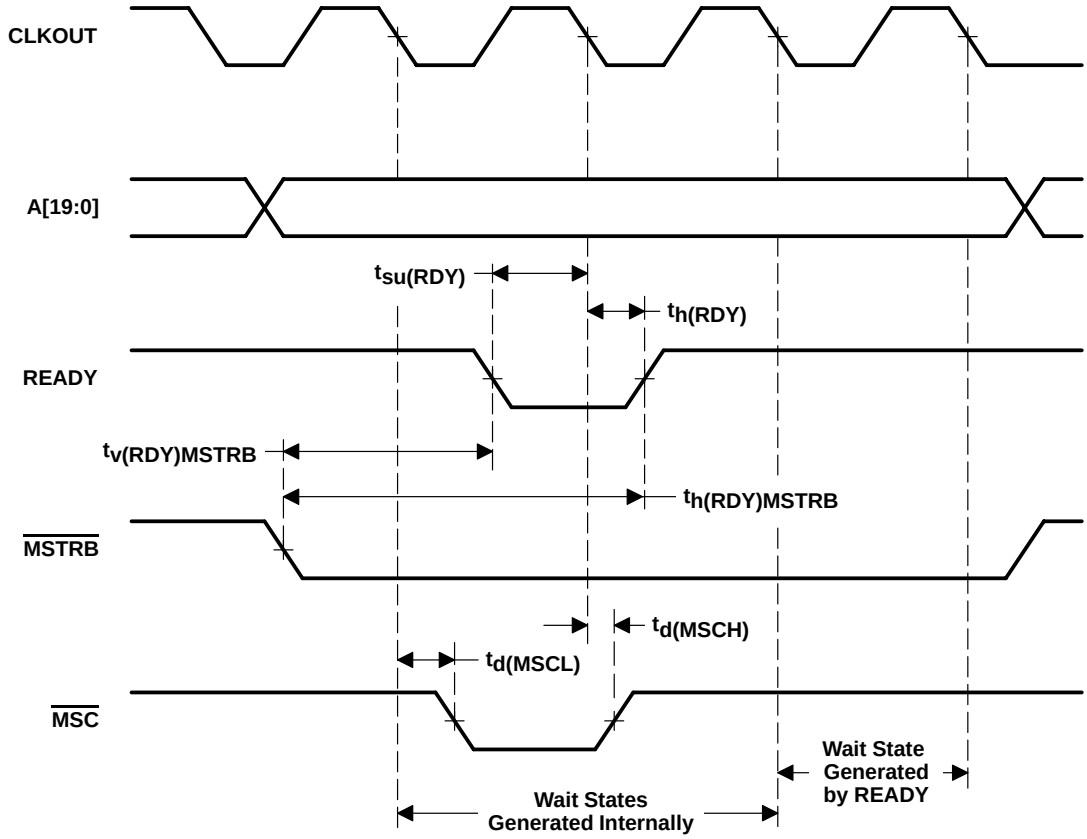
		MIN	MAX	UNIT
$t_{su(RDY)}$	Setup time, READY before CLKOUT low	7		ns
$t_{h(RDY)}$	Hold time, READY after CLKOUT low	–2		ns
$t_{v(RDY)MSTRB}$	Valid time, READY after $\overline{MSTRB}$ low‡		4H–11	ns
$t_{h(RDY)MSTRB}$	Hold time, READY after $\overline{MSTRB}$ low‡	4H–4		ns
$t_{v(RDY)IOSTRB}$	Valid time, READY after $\overline{IOSTRB}$ low‡		5H–11	ns
$t_{h(RDY)IOSTRB}$	Hold time, READY after $\overline{IOSTRB}$ low‡	5H–3		ns

† The hardware wait states can be used only in conjunction with the software wait states to extend the bus cycles. To generate wait states by READY, at least two software wait states must be programmed. READY is not sampled until the completion of the internal software wait states.
‡ These timings are included for reference only. The critical timings for READY are those referenced to CLKOUT.

Table 4–13. Ready Switching Characteristics for Externally Generated Wait States†

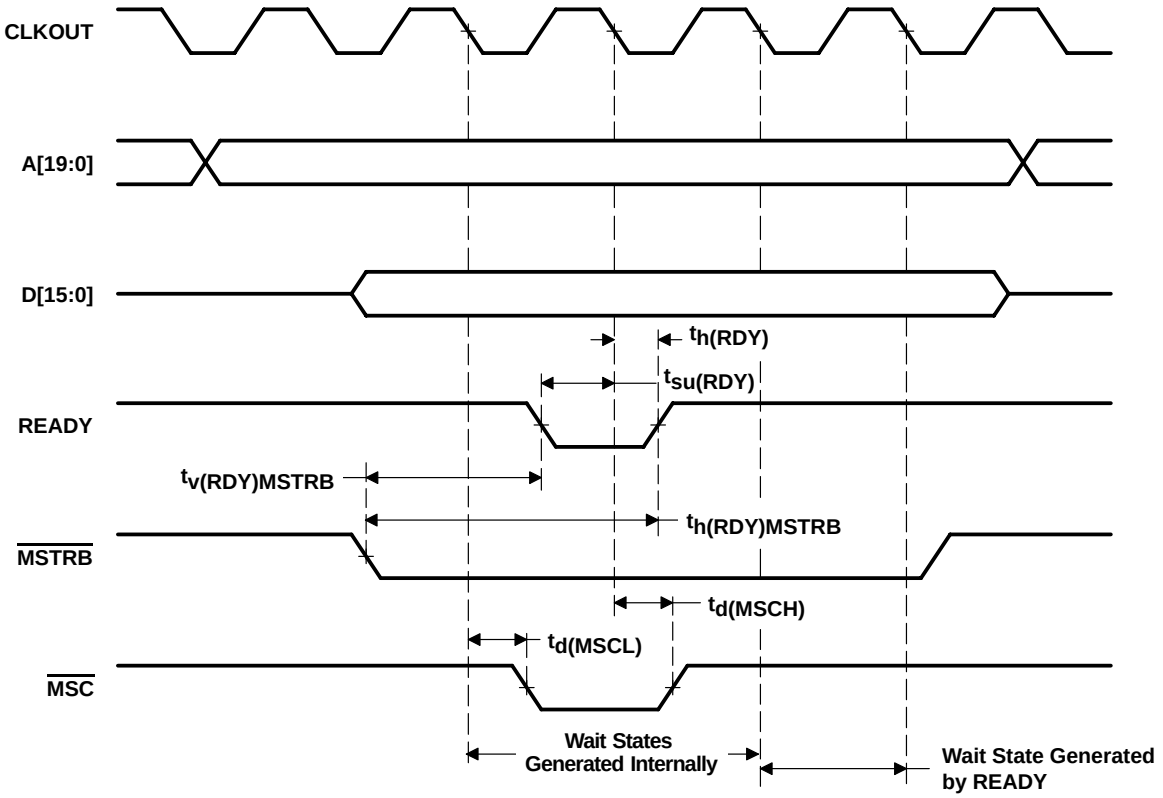
PARAMETER		MIN	MAX	UNIT
$t_{d(MSCL)}$	Delay time, CLKOUT low to $\overline{MSC}$ low	0	8	ns
$t_{d(MSCH)}$	Delay time, CLKOUT low to $\overline{MSC}$ high	– 1	8	ns

† The hardware wait states can be used only in conjunction with the software wait states to extend the bus cycles. To generate wait states by READY, at least two software wait states must be programmed. READY is not sampled until the completion of the internal software wait states.



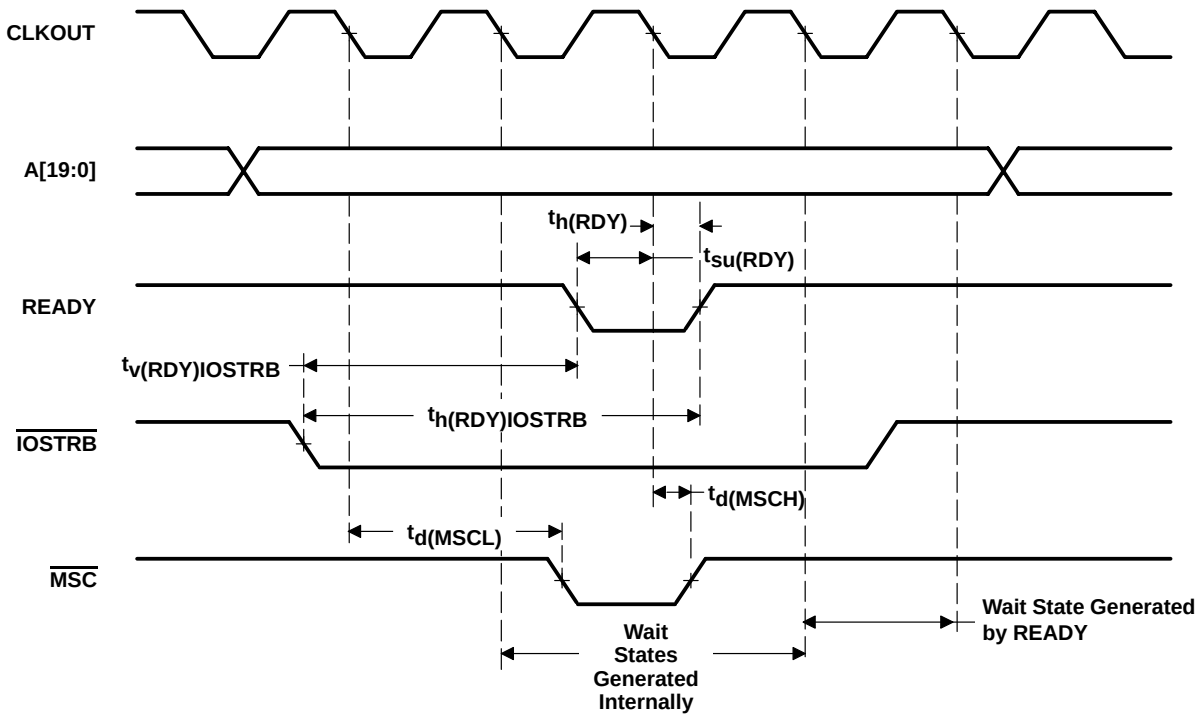
NOTE A: A[19:16] are always driven low during external data space accesses.

Figure 4–9. Memory Read With Externally Generated Wait States



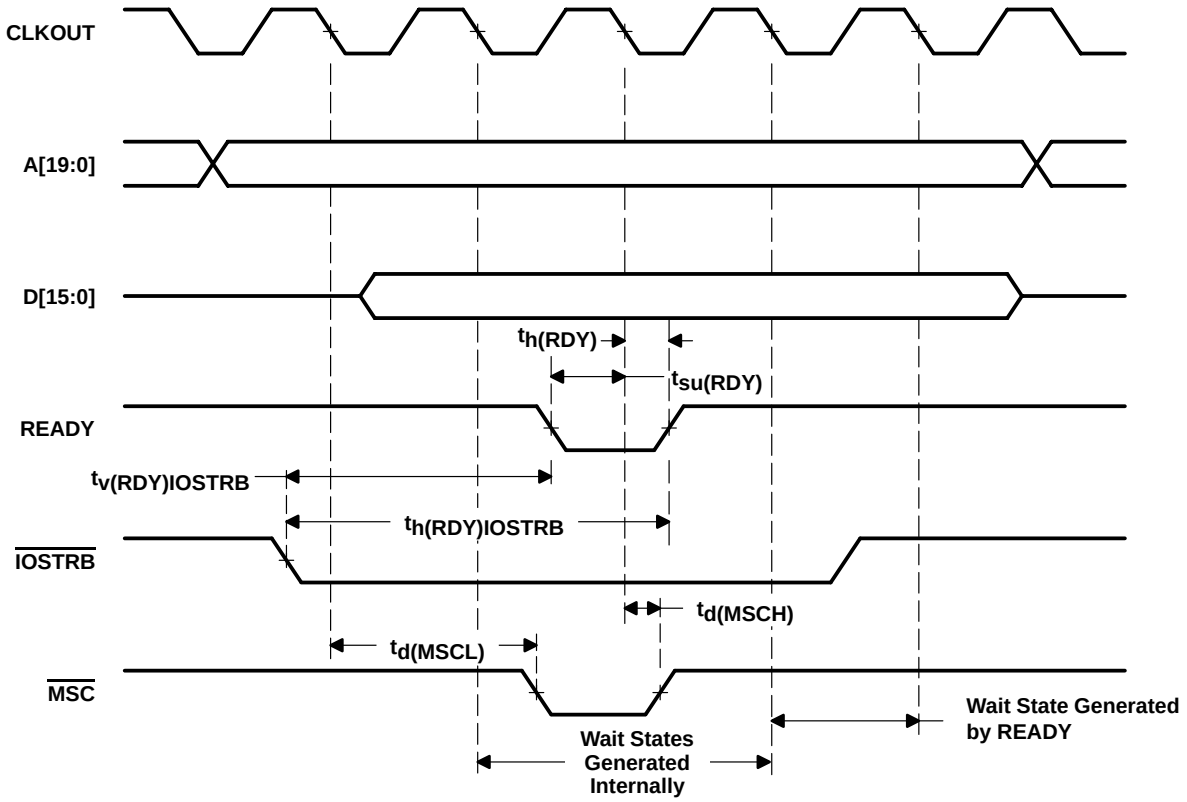
NOTE A: A[19:16] are always driven low during external data space accesses.

Figure 4–10. Memory Write With Externally Generated Wait States



NOTE A: A[19:16] are always driven low during I/O space accesses.

Figure 4–11. I/O Read With Externally Generated Wait States



NOTE A: A[19:16] are always driven low during I/O accesses.

Figure 4–12. I/O Write With Externally Generated Wait States

4.9 $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Timings

Table 4–14 and Table 4–15 assume testing over recommended operating conditions and H = 0.5$t_{c(CO)}$ (see Figure 4–13).

Table 4–14. $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Timing Requirements

		MIN	MAX	UNIT
$t_{w(HOLD)}$	Pulse duration, $\overline{\text{HOLD}}$ low	4H+7		ns
$t_{su(HOLD)}$	Setup time, $\overline{\text{HOLD}}$ low/high before CLKOUT low	7		ns

Table 4–15. $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{dis(CLKL-A)}$	Disable time, address, $\overline{\text{PS}}$, $\overline{\text{DS}}$, $\overline{\text{IS}}$ high impedance from CLKOUT low		3	ns
$t_{dis(CLKL-RW)}$	Disable time, R/$\overline{\text{W}}$ high impedance from CLKOUT low		3	ns
$t_{dis(CLKL-S)}$	Disable time, $\overline{\text{MSTRB}}$, $\overline{\text{IOSTRB}}$ high impedance from CLKOUT low		3	ns
$t_{en(CLKL-A)}$	Enable time, address, $\overline{\text{PS}}$, $\overline{\text{DS}}$, $\overline{\text{IS}}$ from CLKOUT low		2H+7	ns
$t_{en(CLKL-RW)}$	Enable time, R/$\overline{\text{W}}$ enabled from CLKOUT low		2H+7	ns
$t_{en(CLKL-S)}$	Enable time, $\overline{\text{MSTRB}}$, $\overline{\text{IOSTRB}}$ enabled from CLKOUT low		2H+7	ns
$t_{v(HOLDA)}$	Valid time, $\overline{\text{HOLDA}}$ low after CLKOUT low	0	8	ns
	Valid time, $\overline{\text{HOLDA}}$ high after CLKOUT low	0	8	ns
$t_{w(HOLDA)}$	Pulse duration, $\overline{\text{HOLDA}}$ low duration	2H		ns

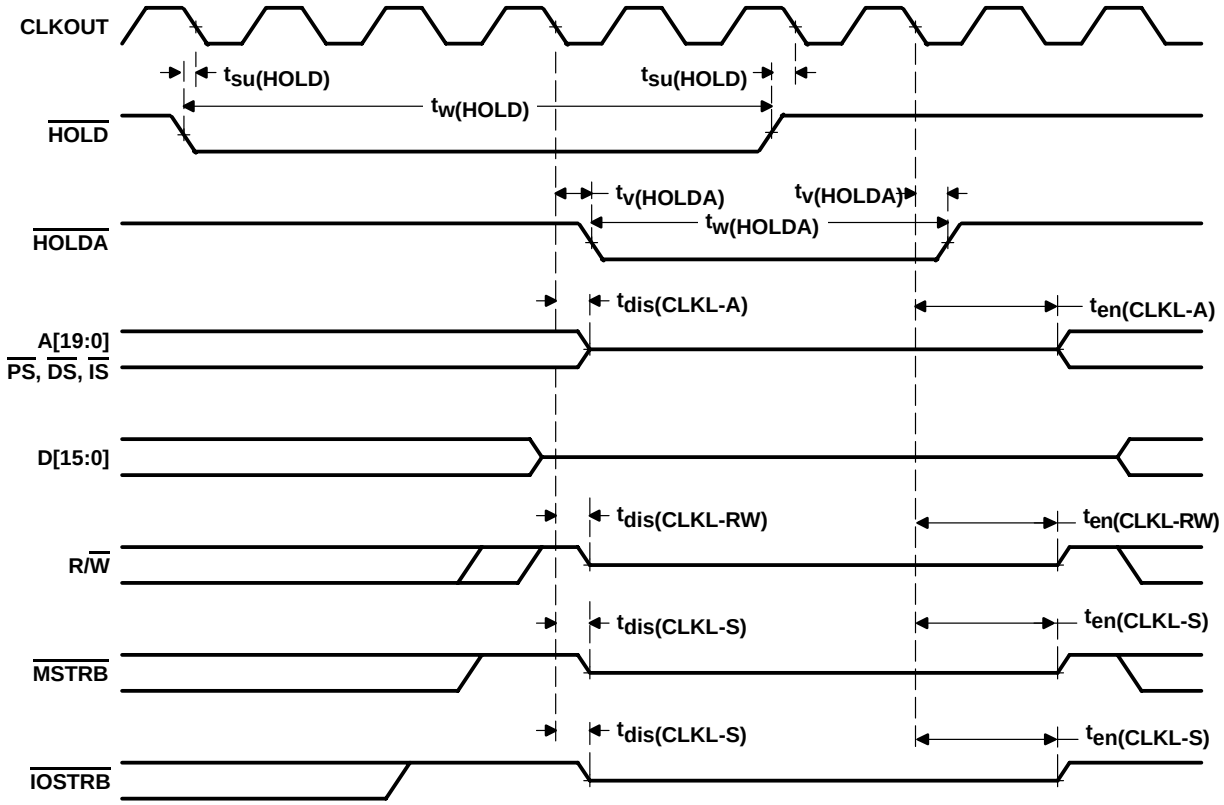


Figure 4–13. $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Timings (HM = 1)

4.10 Reset, $\overline{\text{BIO}}$, Interrupt, and MP/$\overline{\text{MC}}$ Timings

Table 4–16 assumes testing over recommended operating conditions and H = 0.5$t_{c(CO)}$ (see Figure 4–14, Figure 4–15, and Figure 4–16).

Table 4–16. Reset, $\overline{\text{BIO}}$, Interrupt, and MP/$\overline{\text{MC}}$ Timing Requirements

		MIN	MAX	UNIT
$t_{h(RS)}$	Hold time, $\overline{\text{RS}}$ after CLKOUT low	0		ns
$t_{h(BIO)}$	Hold time, $\overline{\text{BIO}}$ after CLKOUT low	–2		ns
$t_{h(INT)}$	Hold time, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$, after CLKOUT low†	–3		ns
$t_{h(MPMC)}$	Hold time, MP/$\overline{\text{MC}}$ after CLKOUT low	0		ns
$t_{w(RSL)}$	Pulse duration, $\overline{\text{RS}}$ low‡§	4H+5		ns
$t_{w(BIO)S}$	Pulse duration, $\overline{\text{BIO}}$ low, synchronous	2H+4		ns
$t_{w(BIO)A}$	Pulse duration, $\overline{\text{BIO}}$ low, asynchronous	4H		ns
$t_{w(INTH)S}$	Pulse duration, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$ high (synchronous)	2H–1		ns
$t_{w(INTH)A}$	Pulse duration, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$ high (asynchronous)	4H		ns
$t_{w(INTL)S}$	Pulse duration, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$ low (synchronous)	2H+1		ns
$t_{w(INTL)A}$	Pulse duration, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$ low (asynchronous)	4H		ns
$t_{w(INTL)WKP}$	Pulse duration, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$ low for IDLE2/IDLE3 wakeup	8		ns
$t_{su(RS)}$	Setup time, $\overline{\text{RS}}$ before X2/CLKIN low¶	5		ns
$t_{su(BIO)}$	Setup time, $\overline{\text{BIO}}$ before CLKOUT low	7	12	ns
$t_{su(INT)}$	Setup time, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$, $\overline{\text{RS}}$ before CLKOUT low	8	12	ns
$t_{su(MPMC)}$	Setup time, MP/$\overline{\text{MC}}$ before CLKOUT low	10		ns

† The external interrupts ($\overline{\text{INT0}}$–$\overline{\text{INT3}}$, $\overline{\text{NMI}}$) are synchronized to the core CPU by way of a two-flip-flop synchronizer which samples these inputs with consecutive falling edges of CLKOUT. The input to the interrupt pins is required to represent a 1-0-0 sequence at the timing that is corresponding to three CLKOUT sampling sequences.

‡ If the PLL mode is selected, then at power-on sequence, or at wakeup from IDLE3, $\overline{\text{RS}}$ must be held low for at least 50 µs to ensure synchronization and lock-in of the PLL.

§ Note that $\overline{\text{RS}}$ may cause a change in clock frequency, therefore changing the value of H.

¶ Divide-by-two mode

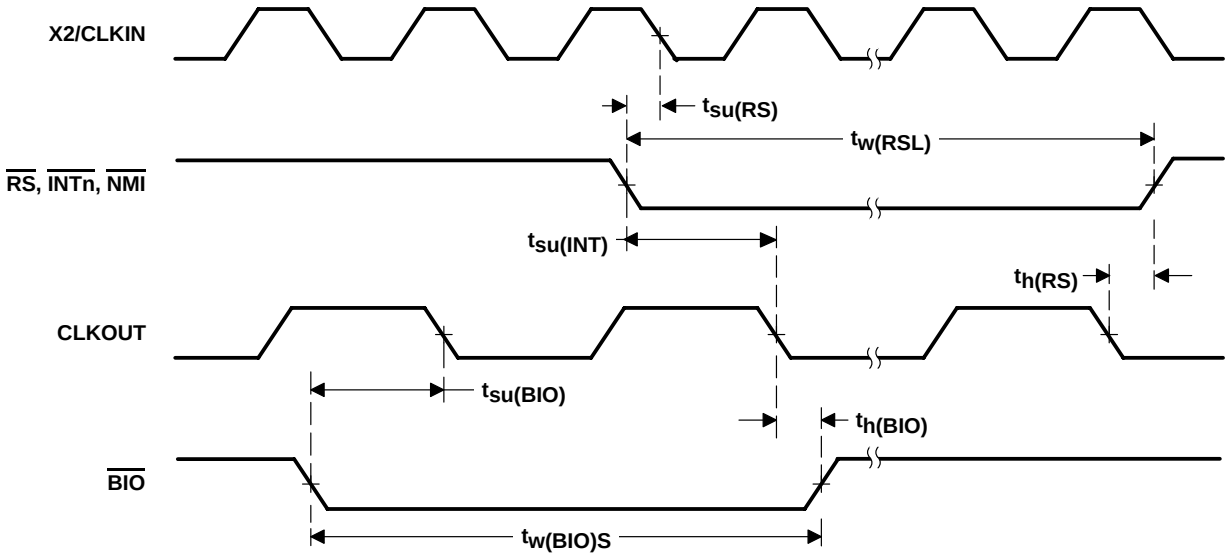


Figure 4–14. Reset and $\overline{\text{BIO}}$ Timings

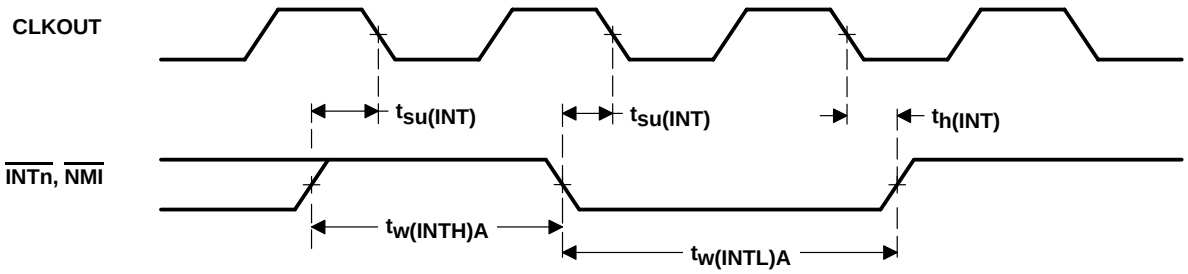


Figure 4–15. Interrupt Timing

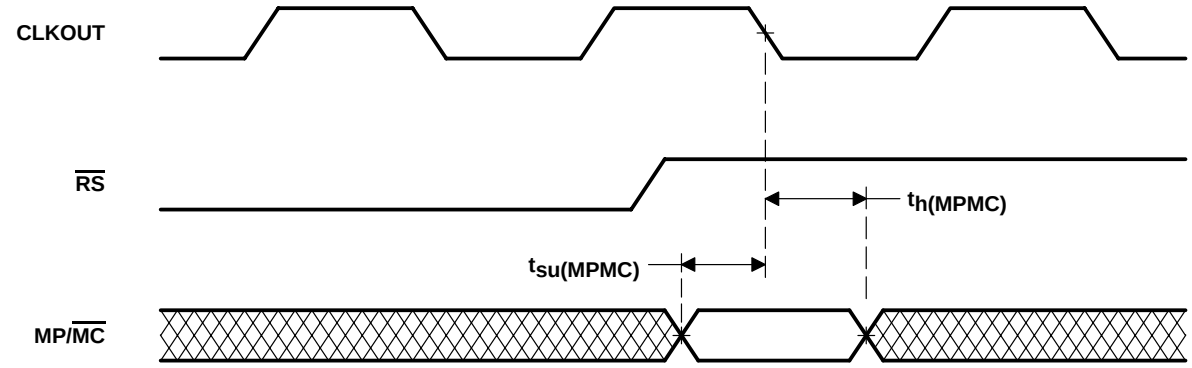


Figure 4–16. MP/$\overline{MC}$ Timing

4.11 Instruction Acquisition ($\overline{IAQ}$) and Interrupt Acknowledge ($\overline{IACK}$) Timings

Table 4–17 assumes testing over recommended operating conditions and H = 0.5$t_{c(CO)}$ (see Figure 4–17).

Table 4–17. Instruction Acquisition ($\overline{IAQ}$) and Interrupt Acknowledge ($\overline{IACK}$) Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{d(CLKL-IAQL)}$	Delay time, CLKOUT low to $\overline{IAQ}$ low	0	9	ns
$t_{d(CLKL-IAQH)}$	Delay time, CLKOUT low to $\overline{IAQ}$ high	0	7	ns
$t_{d(A)IAQ}$	Delay time, address valid to $\overline{IAQ}$ low		2	ns
$t_{d(CLKL-IACKL)}$	Delay time, CLKOUT low to $\overline{IACK}$ low	0	9	ns
$t_{d(CLKL-IACKH)}$	Delay time , CLKOUT low to $\overline{IACK}$ high	1	6	ns
$t_{d(A)IACK}$	Delay time, address valid to $\overline{IACK}$ low		2	ns
$t_{h(A)IAQ}$	Hold time, $\overline{IAQ}$ high after address invalid	–3		ns
$t_{h(A)IACK}$	Hold time, $\overline{IACK}$ high after address invalid	–2		ns
$t_{w(IAQL)}$	Pulse duration, $\overline{IAQ}$ low	2H–2		ns
$t_{w(IACKL)}$	Pulse duration, $\overline{IACK}$ low	2H–1		ns

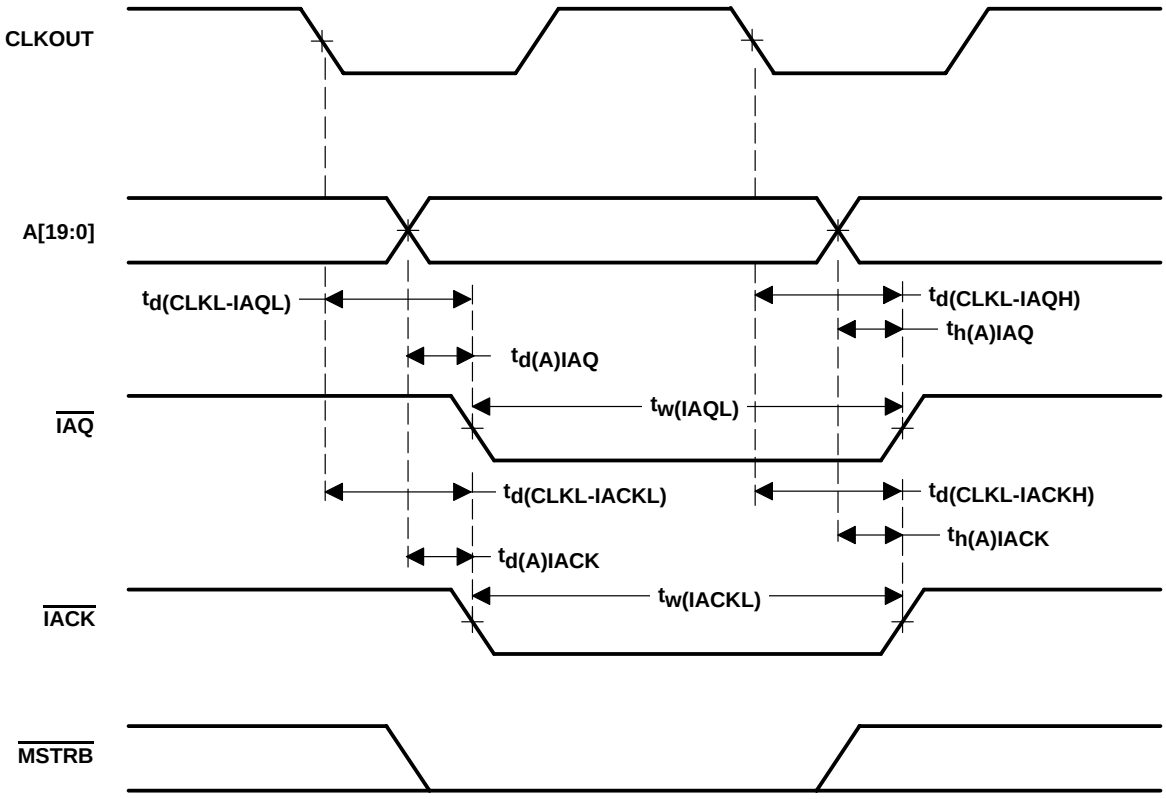


Figure 4–17. $\overline{IAQ}$ and $\overline{IACK}$ Timings

4.12 External Flag (XF) and TOUT Timings

Table 4–18 assumes testing over recommended operating conditions and H = 0.5$t_{c(CO)}$ (see Figure 4–18 and Figure 4–19).

Table 4–18. External Flag (XF) and TOUT Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{d(XF)}$	Delay time, CLKOUT low to XF high	–1	8	ns
	Delay time, CLKOUT low to XF low	–1	8	
$t_{d(TOUTH)}$	Delay time, CLKOUT low to TOUT high	0	11	ns
$t_{d(TOUTL)}$	Delay time, CLKOUT low to TOUT low	0	9	ns
$t_{w(TOUT)}$	Pulse duration, TOUT	2H–1		ns

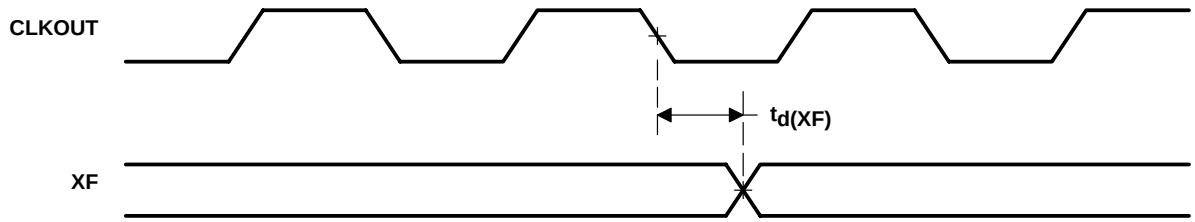


Figure 4–18. XF Timing

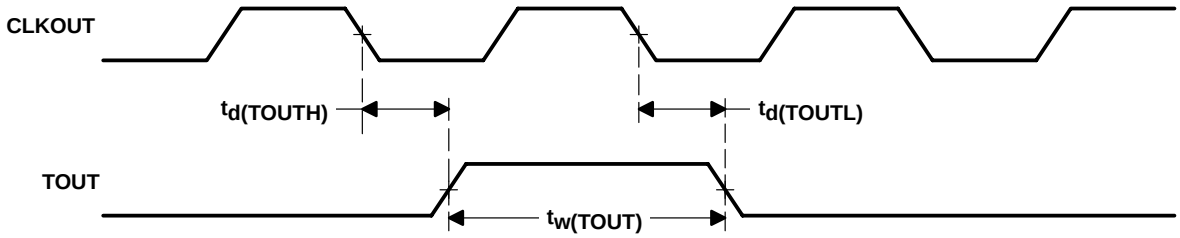


Figure 4–19. TOUT Timing

4.13 Multichannel Buffered Serial Port (McBSP) Timing

4.13.1 McBSP Transmit and Receive Timings

Table 4–19 and Table 4–20 assume testing over recommended operating conditions and H = 0.5$t_{c(CO)}$ (see Figure 4–20 and Figure 4–21).

Table 4–19. McBSP Transmit and Receive Timing Requirements†

			MIN	MAX	UNIT
$t_{c(BCKRX)}$	Cycle time, BCLKR/X	BCLKR/X ext	4H		ns
$t_{w(BCKRX)}$	Pulse duration, BCLKR/X high or BCLKR/X low	BCLKR/X ext	2H–1		ns
$t_{su(BFRH-BCKRL)}$	Setup time, external BFSR high before BCLKR low	BCLKR int	20		ns
		BCLKR ext	0		
$t_{h(BCKRL-BFRH)}$	Hold time, external BFSR high after BCLKR low	BCLKR int	–3		ns
		BCLKR ext	4		
$t_{su(BDRV-BCKRL)}$	Setup time, BDR valid before BCLKR low	BCLKR int	17		ns
		BCLKR ext	0		
$t_{h(BCKRL-BDRV)}$	Hold time, BDR valid after BCLKR low	BCLKR int	0		ns
		BCLKR ext	8		
$t_{su(BFXH-BCKXL)}$	Setup time, external BFSX high before BCLKX low	BCLKX int	20		ns
		BCLKX ext	0		
$t_{h(BCKXL-BFXH)}$	Hold time, external BFSX high after BCLKX low	BCLKX int	–4		ns
		BCLKX ext	5		
$t_{r(BCKRX)}$	Rise time, BCLKR/X	BCLKR/X ext		8	ns
$t_{f(BCKRX)}$	Fall time, BCLKR/X	BCLKR/X ext		8	ns

† CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

Table 4–20. McBSP Transmit and Receive Switching Characteristics†

PARAMETER				MIN	MAX	UNIT
$t_{c(BCKRX)}$	Cycle time, BCLKR/X		BCLKR/X int	4H		ns
$t_{w(BCKRXH)}$	Pulse duration, BCLKR/X high		BCLKR/X int	D – 3‡	D + 2‡	ns
$t_{w(BCKRXL)}$	Pulse duration, BCLKR/X low		BCLKR/X int	C – 3‡	C + 2‡	ns
$t_{d(BCKRH-BFRV)}$	Delay time, BCLKR high to internal BFSR valid		BCLKR int	–3	6	ns
			BCLKR ext	7	13	ns
$t_{d(BCKXH-BFXV)}$	Delay time, BCLKX high to internal BFSX valid		BCLKX int	0	6	ns
			BCLKX ext	5	19	
$t_{dis(BCKXH-BDXHZ)}$	Disable time, BCLKX high to BDX high impedance following last data bit of transfer		BCLKX int	1	6	ns
			BCLKX ext	7	13	
$t_{d(BCKXH-BDXV)}$	Delay time, BCLKX high to BDX valid	DXENA = 0§	BCLKX int	0¶	6	ns
			BCLKX ext	5	19	
$t_{d(BFXH-BDXV)}$	Delay time, BFSX high to BDX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode		BFSX int	1¶	2	ns
			BFSX ext	7	18	

† CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
‡ T = BCLKRX period = (1 + CLKGDV) * 2H
C = BCLKRX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * 2H when CLKGDV is even
D = BCLKRX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * 2H when CLKGDV is even
§ The transmit delay enable (DXENA) and A-bis mode (ABIS) features of the McBSP are not implemented on the TMS320UC5402.
¶ Minimum delay times also represent minimum output hold times.

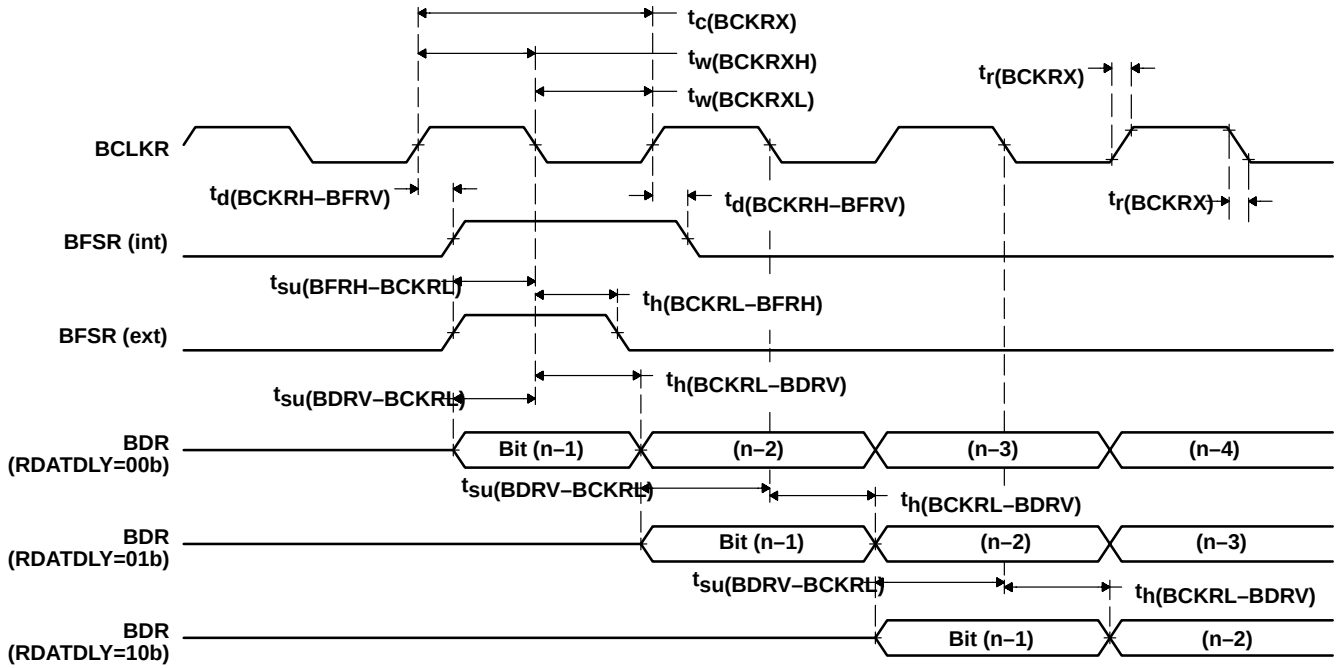


Figure 4–20. McBSP Receive Timings

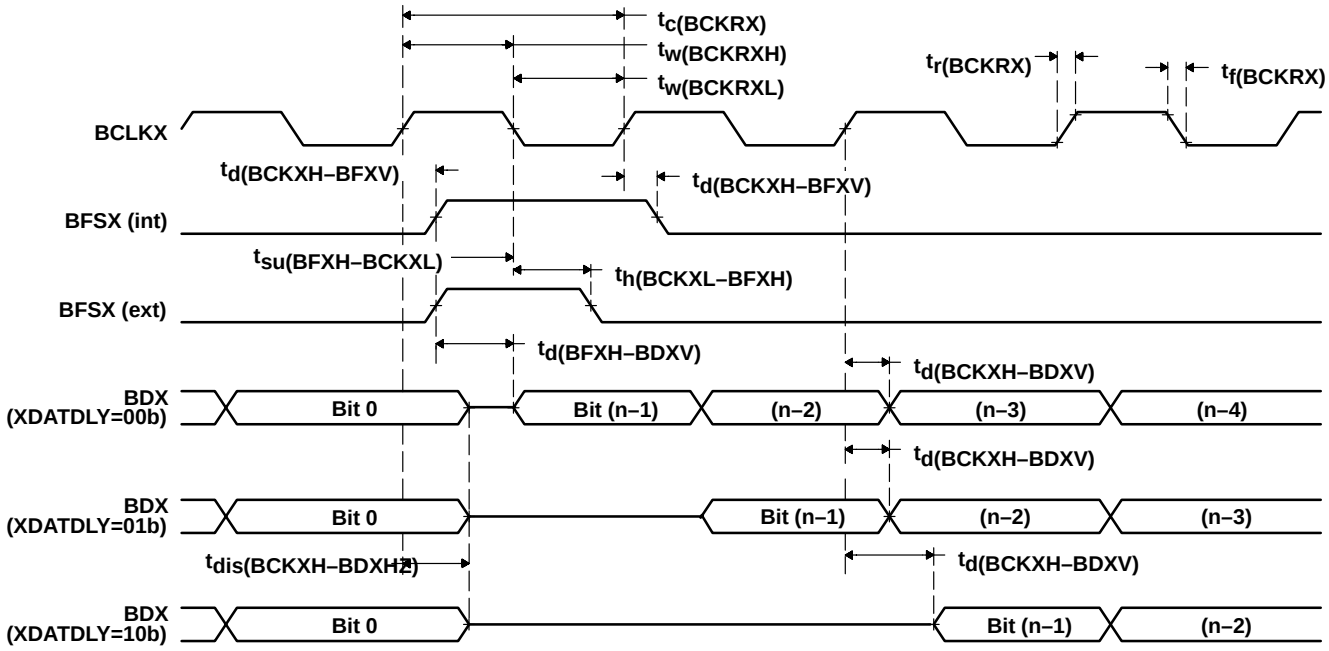


Figure 4–21. McBSP Transmit Timings

4.13.2 McBSP General-Purpose I/O Timing

Table 4–21 and Table 4–22 assume testing over recommended operating conditions (see Figure 4–22).

Table 4–21. McBSP General-Purpose I/O Timing Requirements

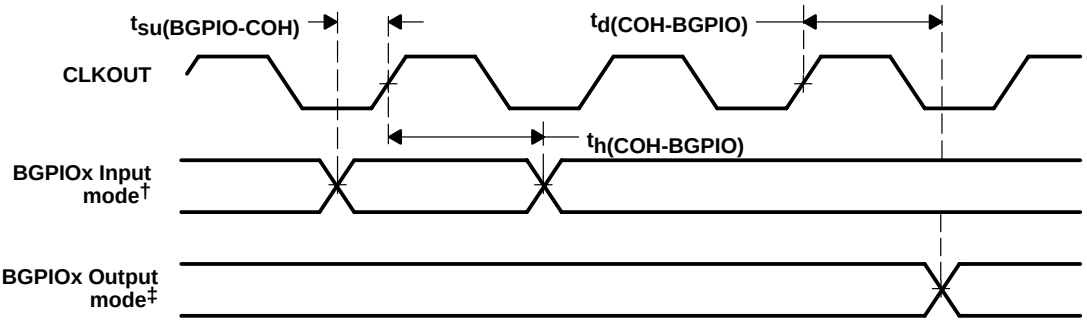
		MIN	MAX	UNIT
$t_{su(BGPIO-COH)}$	Setup time, BGPIOx input mode before CLKOUT high†	9		ns
$t_{h(COH-BGPIO)}$	Hold time, BGPIOx input mode after CLKOUT high†	0		ns

† BGPIOx refers to BCLKRx, BFSRx, BDRx, BCLKXx, or BFSXx when configured as a general-purpose input.

Table 4–22. McBSP General-Purpose I/O Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{d(COH-BGPIO)}$	Delay time, CLKOUT high to BGPIOx output mode‡	0	5	ns

‡ BGPIOx refers to BCLKRx, BFSRx, BCLKXx, BFSXx, or BDXx when configured as a general-purpose output.



† BGPIOx refers to BCLKRx, BFSRx, BDRx, BCLKXx, or BFSXx when configured as a general-purpose input.
‡ BGPIOx refers to BCLKRx, BFSRx, BCLKXx, BFSXx, or BDXx when configured as a general-purpose output.

Figure 4–22. McBSP General-Purpose I/O Timings

4.13.3 McBSP as SPI Master or Slave Timing

Table 4–23 to Table 4–30 assume testing over recommended operating conditions and H = $0.5t_{c(CO)}$ (see Figure 4–23, Figure 4–24, Figure 4–25, and Figure 4–26).

Table 4–23. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 0)†

		MASTER		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
$t_{su(BDRV-BCKXL)}$	Setup time, BDR valid before BCLKX low	16		– 12H		ns
$t_{h(BCKXL-BDRV)}$	Hold time, BDR valid after BCLKX low	4		12H + 5		ns
$t_{su(BFXL-BCKXH)}$	Setup time, BFSX low before BCLKX high			10		ns
$t_{c(BCKX)}$	Cycle time, BCLKX	12H		32H		ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

Table 4–24. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 0)†

PARAMETER		MASTER‡		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
$t_{h(BCKXL-BFXL)}$	Hold time, BFSX low after BCLKX low§	T – 4	T + 5			ns
$t_{d(BFXL-BCKXH)}$	Delay time, BFSX low to BCLKX high¶	C – 6	C + 4			ns
$t_{d(BCKXH-BDXV)}$	Delay time, BCLKX high to BDX valid	–3	7	6H + 6	10H + 20	ns
$t_{dis(BCKXL-BDXHZ)}$	Disable time, BDX high impedance following last data bit from BCLKX low	C – 2	C + 3			ns
$t_{dis(BFXH-BDXHZ)}$	Disable time, BDX high impedance following last data bit from BFSX high			2H+ 8	6H + 21	ns
$t_{d(BFXL-BDXV)}$	Delay time, BFSX low to BDX valid			4H –3	8H + 21	ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ T = BCLKX period = (1 + CLKGDV) * 2H
C = BCLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * 2H when CLKGDV is even
§ FSRP = FSXP = 1. As a SPI master, BFSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on BFSX and BFSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
¶ BFSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (BCLKX).

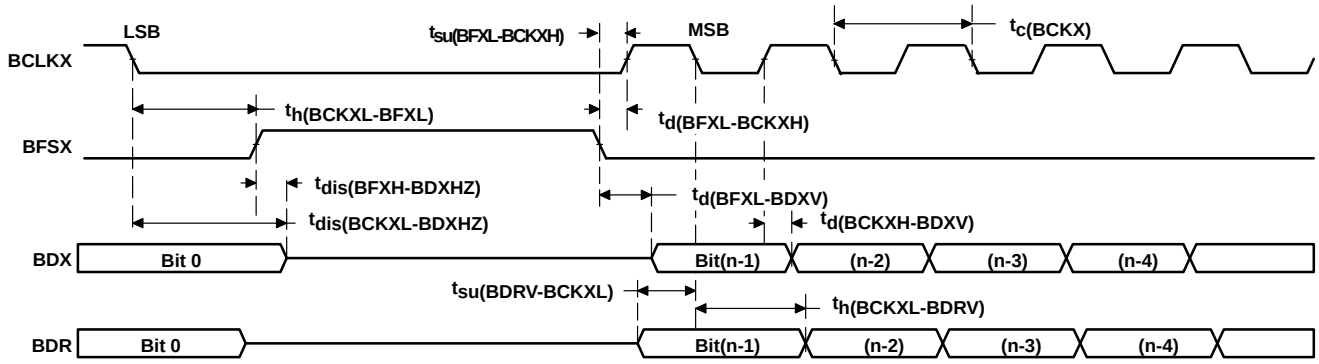


Figure 4–23. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0

Table 4–25. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 0)†

		MASTER		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
$t_{su(BDRV-BCKXH)}$	Setup time, BDR valid before BCLKX high	16		– 12H		ns
$t_{h(BCKXH-BDRV)}$	Hold time, BDR valid after BCLKX high	4		12H + 5		ns
$t_{su(BFXL-BCKXH)}$	Setup time, BFSX low before BCLKX high			10		ns
$t_{c(BCKX)}$	Cycle time, BCLKX	12H		32H		ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

Table 4–26. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 0)†

PARAMETER		MASTER‡		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
$t_{h(BCKXL-BFXL)}$	Hold time, BFSX low after BCLKX low§	C –4	C + 5			ns
$t_{d(BFXL-BCKXH)}$	Delay time, BFSX low to BCLKX high¶	T – 6	T + 4			ns
$t_{d(BCKXL-BDXV)}$	Delay time, BCLKX low to BDX valid	–3	7	6H + 6	10H + 20	ns
$t_{dis(BCKXL-BDXHZ)}$	Disable time, BDX high impedance following last data bit from BCLKX low	0	6	6H +7	10H + 21	ns
$t_{d(BFXL-BDXV)}$	Delay time, BFSX low to BDX valid	D – 2	D + 4	4H –3	8H + 21	ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

‡ T = BCLKX period = (1 + CLKGDV) * 2H
C = BCLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * 2H when CLKGDV is even
D = BCLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * 2H when CLKGDV is even

§ FSRP = FSXP = 1. As a SPI master, BFSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on BFSX and BFSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP

¶ BFSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (BCLKX).

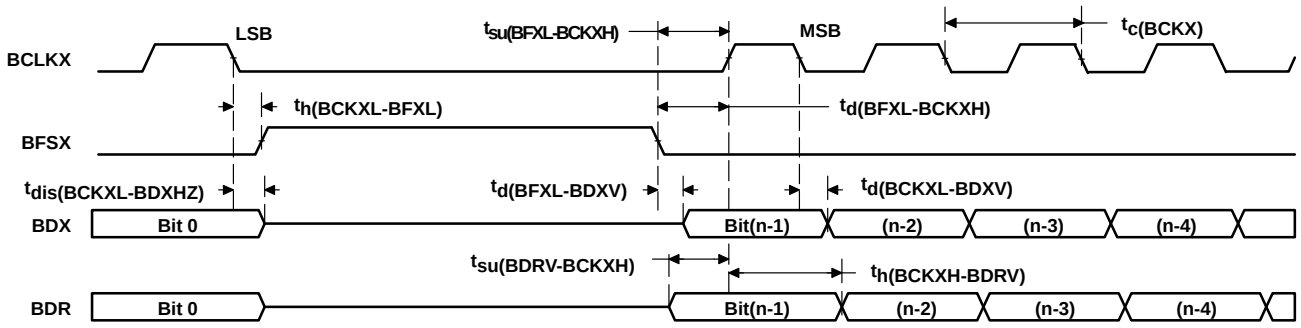


Figure 4–24. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0

Table 4–27. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 1)†

		MASTER		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
$t_{su(BDRV-BCKXH)}$	Setup time, BDR valid before BCLKX high	16		– 12H		ns
$t_{h(BCKXH-BDRV)}$	Hold time, BDR valid after BCLKX high	4		12H + 5		ns
$t_{su(BFXL-BCKXL)}$	Setup time, BFSX low before BCLKX low			10		ns
$t_{c(BCKX)}$	Cycle time, BCLKX	12H		32H		ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

Table 4–28. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 1)†

PARAMETER		MASTER‡		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
$t_{h(BCKXH-BFXL)}$	Hold time, BFSX low after BCLKX high§	T – 4	T + 5			ns
$t_{d(BFXL-BCKXL)}$	Delay time, BFSX low to BCLKX low¶	D – 6	D + 4			ns
$t_{d(BCKXL-BDXV)}$	Delay time, BCLKX low to BDX valid	– 3	7	6H + 6	10H + 20	ns
$t_{dis(BCKXH-BDXHZ)}$	Disable time, BDX high impedance following last data bit from BCLKX high	D – 2	D + 3			ns
$t_{dis(BFXH-BDXHZ)}$	Disable time, BDX high impedance following last data bit from BFSX high			2H + 7	6H + 21	ns
$t_{d(BFXL-BDXV)}$	Delay time, BFSX low to BDX valid			4H – 3	8H + 21	ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ T = BCLKX period = (1 + CLKGDV) * 2H
D = BCLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * 2H when CLKGDV is even
§ FSRP = FSXP = 1. As a SPI master, BFSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on BFSX and BFSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
¶ BFSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (BCLKX).

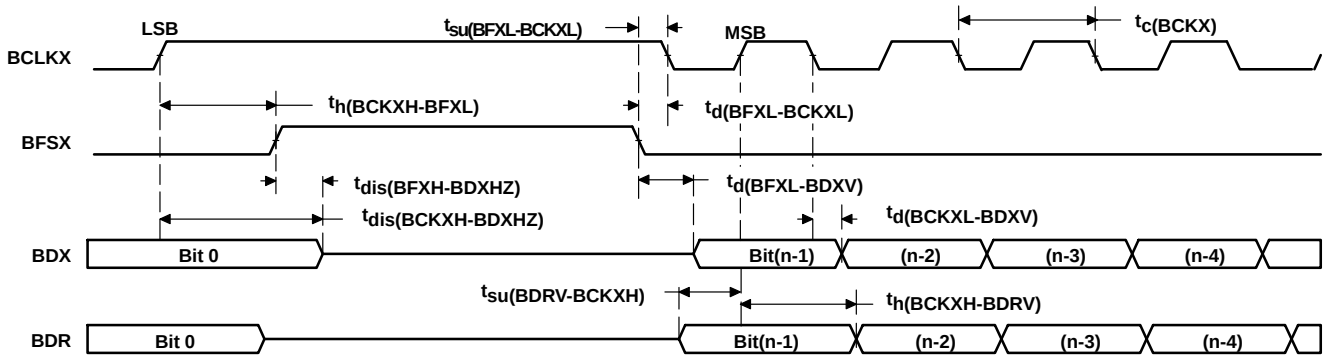


Figure 4–25. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1

Table 4–29. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 1)†

		MASTER		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
$t_{su(BDRV-BCKXL)}$	Setup time, BDR valid before BCLKX low	16		– 12H		ns
$t_{h(BCKXL-BDRV)}$	Hold time, BDR valid after BCLKX low	4		12H + 5		ns
$t_{su(BFXL-BCKXL)}$	Setup time, BFSX low before BCLKX low			10		ns
$t_{c(BCKX)}$	Cycle time, BCLKX	12H		32H		ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

Table 4–30. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 1)†

PARAMETER		MASTER‡		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
$t_{h(BCKXH-BFXL)}$	Hold time, BFSX low after BCLKX high§	D – 4	D + 5			ns
$t_{d(BFXL-BCKXL)}$	Delay time, BFSX low to BCLKX low¶	T – 6	T + 4			ns
$t_{d(BCKXH-BDXV)}$	Delay time, BCLKX high to BDX valid	– 3	7	6H + 6	10H + 20	ns
$t_{dis(BCKXH-BDXHZ)}$	Disable time, BDX high impedance following last data bit from BCLKX high	0	6	6H +7	10H + 21	ns
$t_{d(BFXL-BDXV)}$	Delay time, BFSX low to BDX valid	C – 2	C + 4	4H – 3	8H + 21	ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

‡ T = BCLKX period = (1 + CLKGDV) * 2H
C = BCLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * 2H when CLKGDV is even
D = BCLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * 2H when CLKGDV is even

§ FSRP = FSXP = 1. As a SPI master, BFSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on BFSX and BFSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP

¶ BFSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (BCLKX).

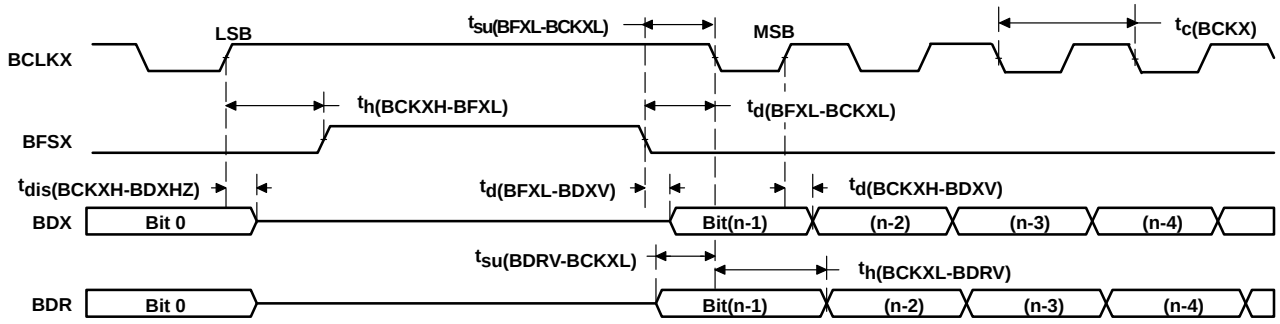


Figure 4–26. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1

4.14 Host-Port Interface Timing (HPI8)

Table 4–31 and Table 4–32 assume testing over recommended operating conditions and $H = 0.5t_{c(CO)}$ (see Figure 4–27 through Figure 4–30). In the following tables, DS refers to the logical OR of $\overline{HCS}$, $\overline{HDS1}$, and $\overline{HDS2}$. HD refers to any of the HPI data bus pins (HD0, HD1, HD2, etc.). HAD stands for HCNTL0, HCNTL1, and HR/$\overline{W}$. GPIO refers to the HD pins when they are configured as general-purpose input/outputs.

NOTE: During all cycles, DS should not be driven high to complete the cycle until HRDY is high. In the case of a read cycle, HDx should also be valid before rising DS.

Table 4–31. HPI8 Mode Timing Requirements

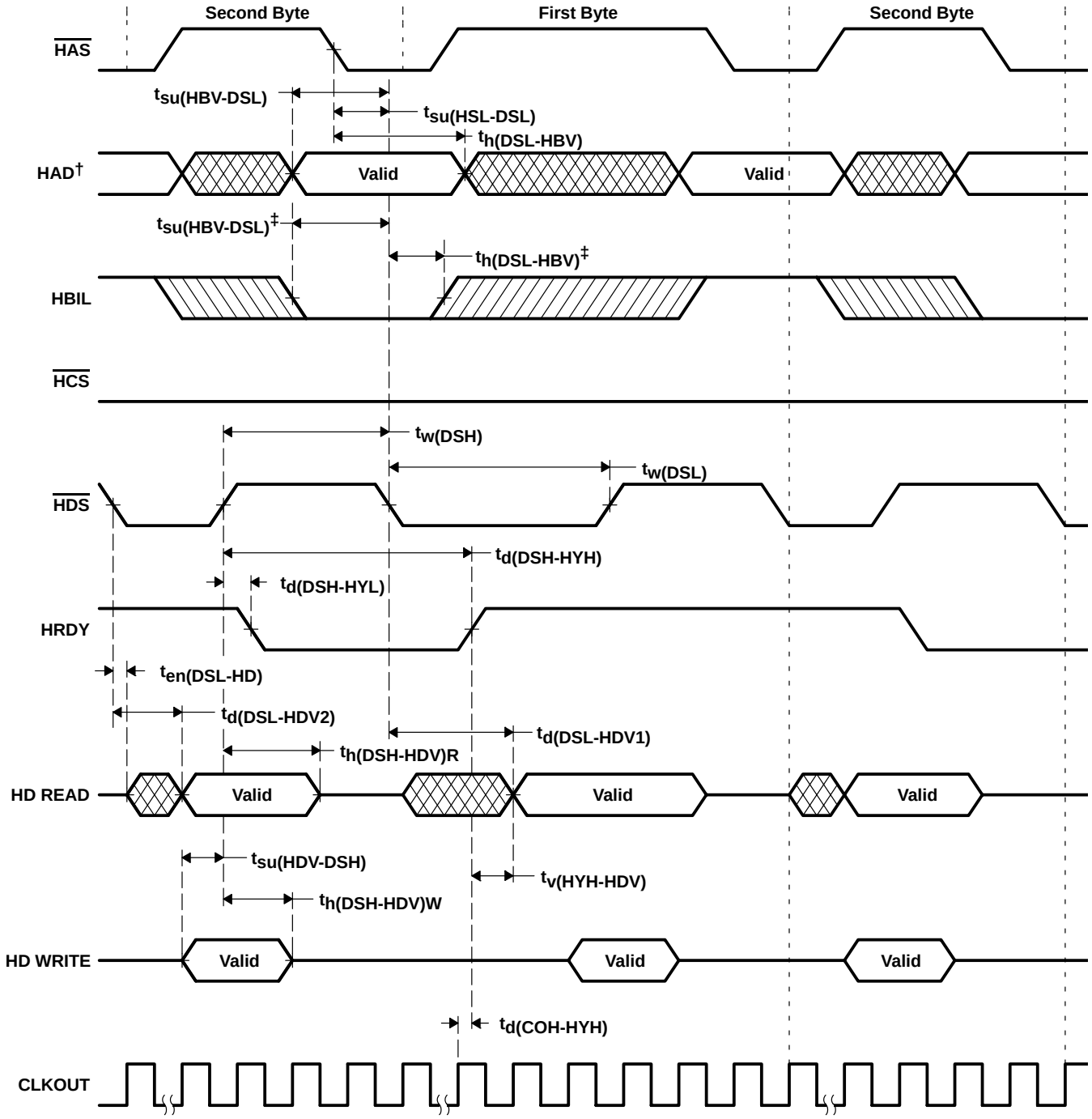
		MIN	MAX	UNIT
$t_{su(HBV-DSL)}$	Setup time, HBIL valid before DS low	5		ns
$t_{h(DSL-HBV)}$	Hold time, HBIL valid after DS low	6		ns
$t_{su(HSL-DSL)}$	Setup time, $\overline{HAS}$ low before DS low	5		ns
$t_{w(DSL)}$	Pulse duration, DS low	20		ns
$t_{w(DSH)}$	Pulse duration, DS high	10		ns
$t_{su(HDV-DSH)}$	Setup time, HDx valid before DS high, HPI write	12		ns
$t_{h(DSH-HDV)W}$	Hold time, HDx valid after DS high, HPI write	8		ns
$t_{su(GPIO-COH)}$	Setup time, HDx input valid before CLKOUT high, HDx configured as general-purpose input	9		ns
$t_{h(GPIO-COH)}$	Hold time, HDx input valid after CLKOUT high, HDx configured as general-purpose input	–3		ns

Table 4–32. HPI8 Mode Switching Characteristics

PARAMETER			MIN	MAX	UNIT
$t_{en(DSL-HD)}$	Enable time, HD driven from DS low		5	21	ns
$t_{d(DSL-HDV1)}$	Delay time, DS low to HDx valid for first byte of an HPI read	Case 1a: Memory accesses when DMAC is active in 16-bit mode and $t_{w(DSH)} < 18H$†		18H + 21 – $t_{w(DSH)}$	ns
		Case 1b: Memory accesses when DMAC is active in 16-bit mode and $t_{w(DSH)} \geq 18H$†		21	
		Case 1c: Memory access when DMAC is active in 32-bit mode and $t_{w(DSH)} < 26H$†		26H + 21 – $t_{w(DSH)}$	
		Case 1d: Memory access when DMAC is active in 32-bit mode and $t_{w(DSH)} \geq 26H$†		21	
		Case 2a: Memory accesses when DMAC is inactive and $t_{w(DSH)} < 10H$†		10H + 21 – $t_{w(DSH)}$	
		Case 2b: Memory accesses when DMAC is inactive and $t_{w(DSH)} \geq 10H$†		21	
		Case 3: Register accesses		21	
$t_{d(DSL-HDV2)}$	Delay time, DS low to HDx valid for second byte of an HPI read			21	ns
$t_{h(DSH-HDV)R}$	Hold time, HDx valid after DS high, for a HPI read		5	9	ns
$t_{v(HYH-HDV)}$	Valid time, HDx valid after HRDY high			12	
$t_{d(DSH-HYL)}$	Delay time, DS high to HRDY low (see Note 1)			21	ns
$t_{d(DSH-HYH)}$	Delay time, DS high to HRDY high	Case 1a: Memory accesses when DMAC is active in 16-bit mode†		18H + 21	ns
		Case 1b: Memory accesses when DMAC is active in 32-bit mode†		26H + 21	ns
		Case 2: Memory accesses when DMAC is inactive†		10H + 21	ns
		Case 3: Write accesses to HPIC register (see Note 2)		6H + 21	
$t_{d(HCS-HRDY)}$	Delay time, $\overline{HCS}$ low/high to HRDY low/high			19	ns
$t_{d(COH-HYH)}$	Delay time, CLKOUT high to HRDY high			5	ns
$t_{d(COH-HTX)}$	Delay time, CLKOUT high to $\overline{HINT}$ change			5	ns
$t_{d(COH-GPIO)}$	Delay time, CLKOUT high to HDx output change. HDx is configured as a general-purpose output.			9	ns

NOTES: 1. The HRDY output is always high when the $\overline{HCS}$ input is high, regardless of DS timings.
2. This timing applies to the first byte of an access, when writing a one to the DSPINT bit or HINT bit of the HPIC register. All other writes to the HPIC occur asynchronously, and do not cause HRDY to be deasserted.

† DMAC stands for direct memory access (DMA) controller. The HPI8 shares the internal DMA bus with the DMAC, thus HPI8 access times are affected by DMAC activity.



† HAD refers to HCNTL0, HCNTL1, and HR/$\overline{W}$.
‡ When $\overline{HAS}$ is not used ($\overline{HAS}$ always high)

Figure 4–27. Using $\overline{HDS}$ to Control Accesses ($\overline{HCS}$ Always Low)

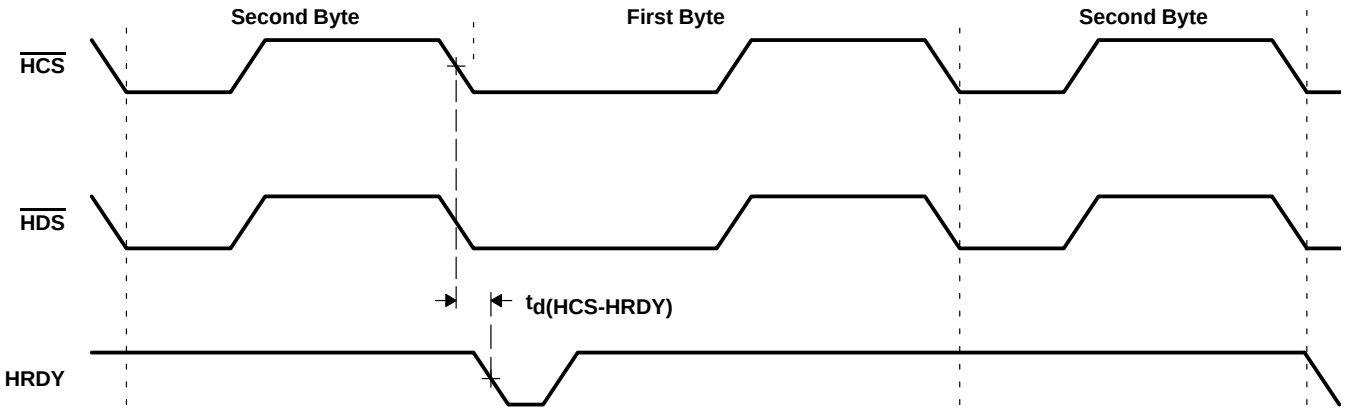


Figure 4–28. Using $\overline{\text{HCS}}$ to Control Accesses

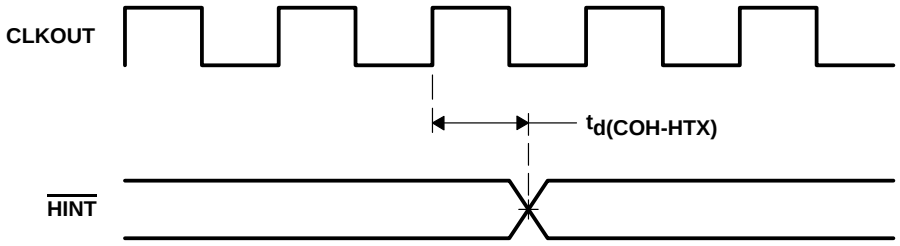
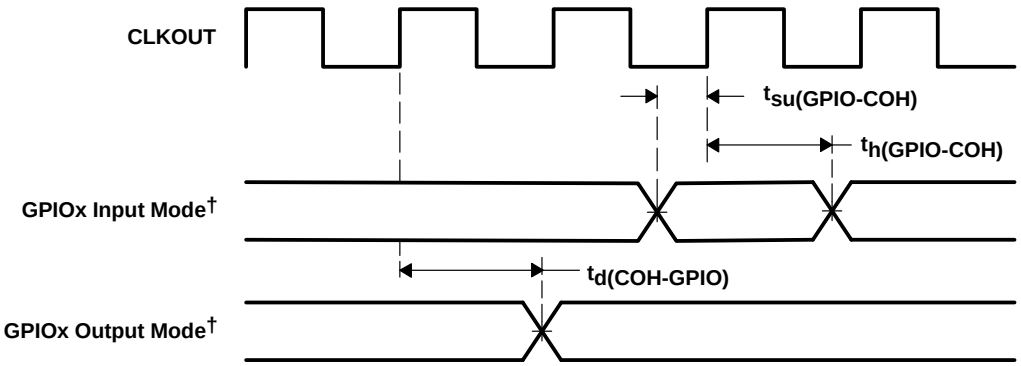


Figure 4–29. $\overline{\text{HINT}}$ Timing



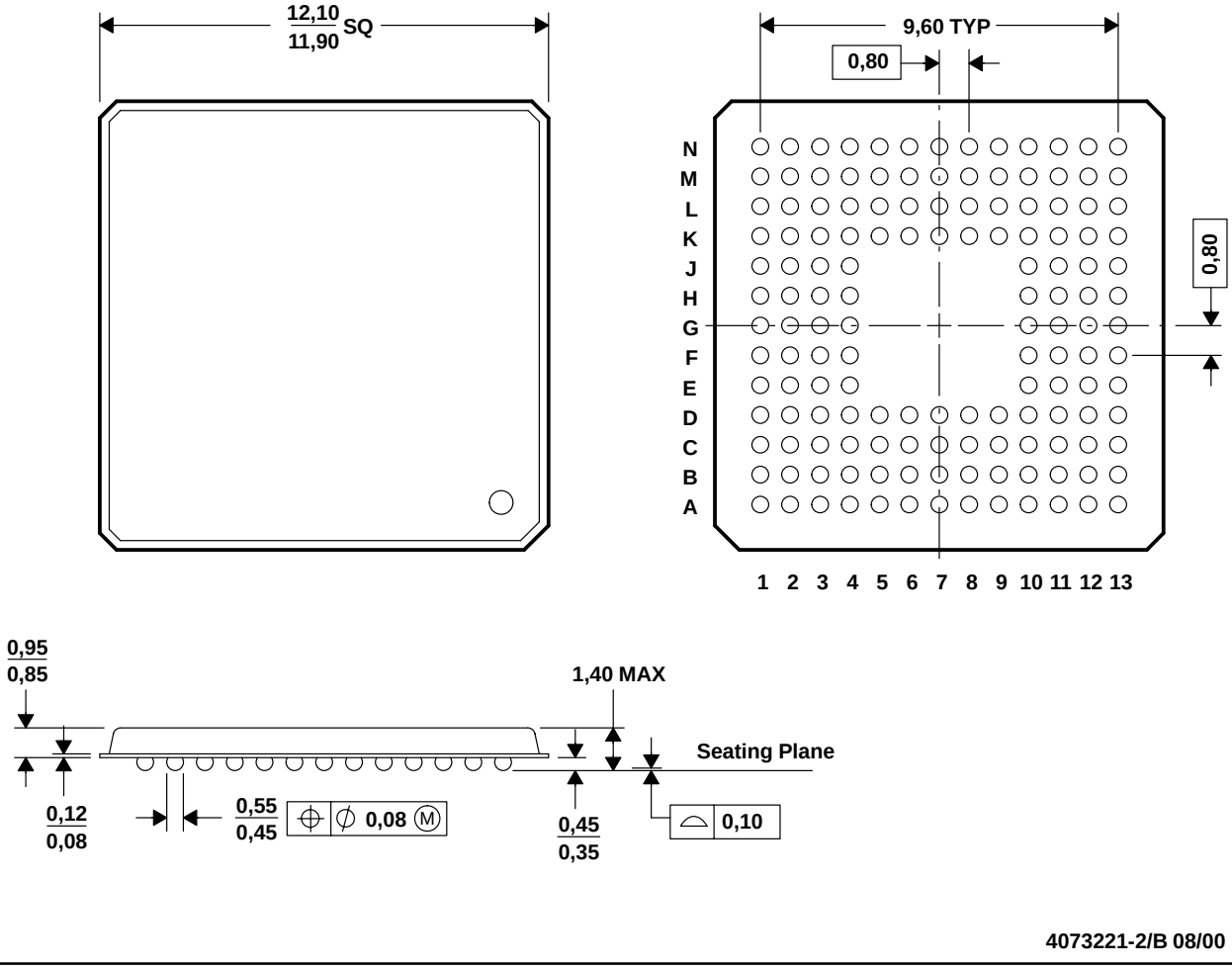
† GPIOx refers to HD0, HD1, HD2, ...HD7, when the HD bus is configured for general-purpose input/output (I/O).

Figure 4–30. GPIOx† Timings

5 Mechanical Data

5.1 Ball Grid Array Mechanical Data

GGU (S-PBGA-N144) **PLASTIC BALL GRID ARRAY**



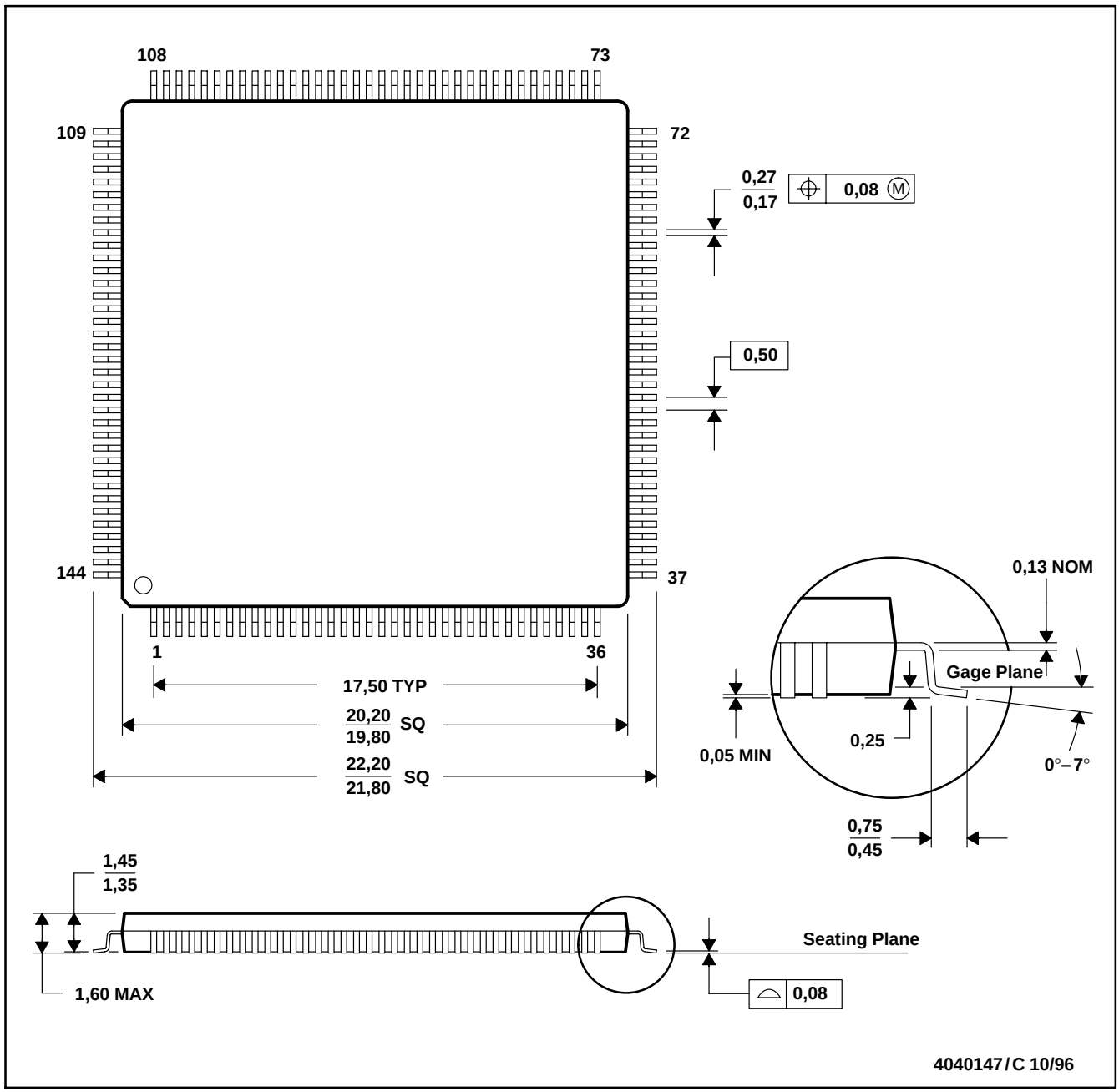
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

Figure 5–1. TMS320UC5402 144-Ball MicroStar BGA™ Plastic Ball Grid Array

MicroStar BGA is a trademark of Texas Instruments.

5.2 Low-Profile Quad Flatpack Mechanical Data

PGE (S-PQFP-G144) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

Figure 5–2. TMS320UC5402 144-Pin Low-Profile Quad Flatpack