Winbond Electronics Corp.

128K × 8 CMOS STATIC RAM

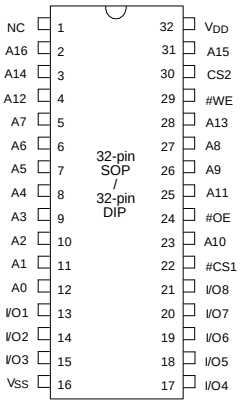
GENERAL DESCRIPTION

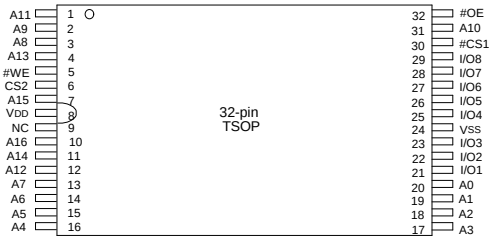
The W24100 is a normal-speed, very low-power CMOS static RAM organized as 131072 × 8 bits that operates on a single 5-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

FEATURES

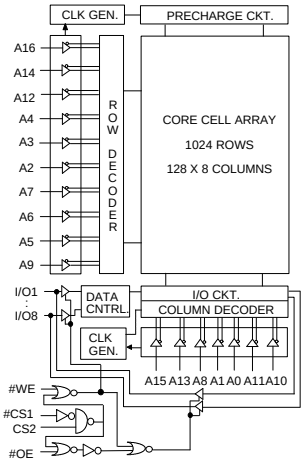
- Low power consumption:
  - Active: 385 mW (max.)
- Access time: 70 nS
- Single 5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 2V (min.)
- Package: 32-pin 600 mil DIP, 32-pin 450 mil SOP, standard type one TSOP (8 mm × 20 mm) and small type one TSOP (8 mm × 13.4 mm)

PIN CONFIGURATIONS





BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A16	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
#CS1, CS2	Chip Select Input
#WE	Write Enable Input
#OE	Output Enable Input
VDD	Power Supply
VSS	Ground
NC	No Connection

TRUTH TABLE

#CS1	CS2	#OE	#WE	MODE	I/O1 - I/O8	VDD CURRENT
H	X	X	X	Not Selected	High Z	ISB, ISB1
X	L	X	X	Not Selected	High Z	ISB, ISB1
L	H	H	H	Output Disable	High Z	IDD
L	H	L	H	Read	Data Out	IDD
L	H	X	L	Write	Data In	IDD

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER		RATING	UNIT
Supply Voltage to VSS Potential		-0.5 to +7.0	V
Input/Output to VSS Potential		-0.5 to VDD +0.5	V
Allowable Power Dissipation		1.0	W
Storage Temperature		-65 to +150	°C
Operating Temperature	L/LL	0 to 70	°C
	LE	-20 to 85	

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(VDD = 5V ±10%; VSS = 0V; TA (°C) = 0 to 70 for LL, -20 to 85 for LE)

PARAMETER	SYM.	TEST CONDITIONS		MIN.	TYP.*	MAX.	UNIT
Input Low Voltage	VIL	-		-0.5	-	+0.8	V
Input High Voltage	VIH	-		+2.2	-	VDD +0.5	V
Input Leakage Current	ILI	VIN = VSS to VDD		-1	-	+1	µA
Output Leakage Current	ILO	VI/O = VSS to VDD, #CS1 = VIH (min.) or #OE = VIH (min.) or #WE = VIL (max.)		-1	-	+1	µA
Output Low Voltage	VOL	IOL = +2.1 mA		-	-	0.4	V
Output High Voltage	VOH	IOH = -1.0 mA		2.4	-	-	V
Operating Power Supply Current	IDD	#CS1 = VIL (max.) and CS2 = VIH (min.), I/O = 0 mA Cycle = min., Duty = 100%		-	-	70	mA
Standby Power Supply Current	ISB	#CS1 = VIH (min.), Cycle = min. Duty = 100%		-	-	3	mA
	ISB1	#CS1 ≥ VDD -0.2V or	LL/LE	-	-	50/70	µA
		CS2 ≤ 0.2V	L	-	-	100	

DC Characteristics, Continued

Note: Typical parameter is measured under ambient temperature T_A = 25° C and V_{DD} = 5V.

CAPACITANCE

(V_{DD} = 5 V, T_A = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0V	8	pF

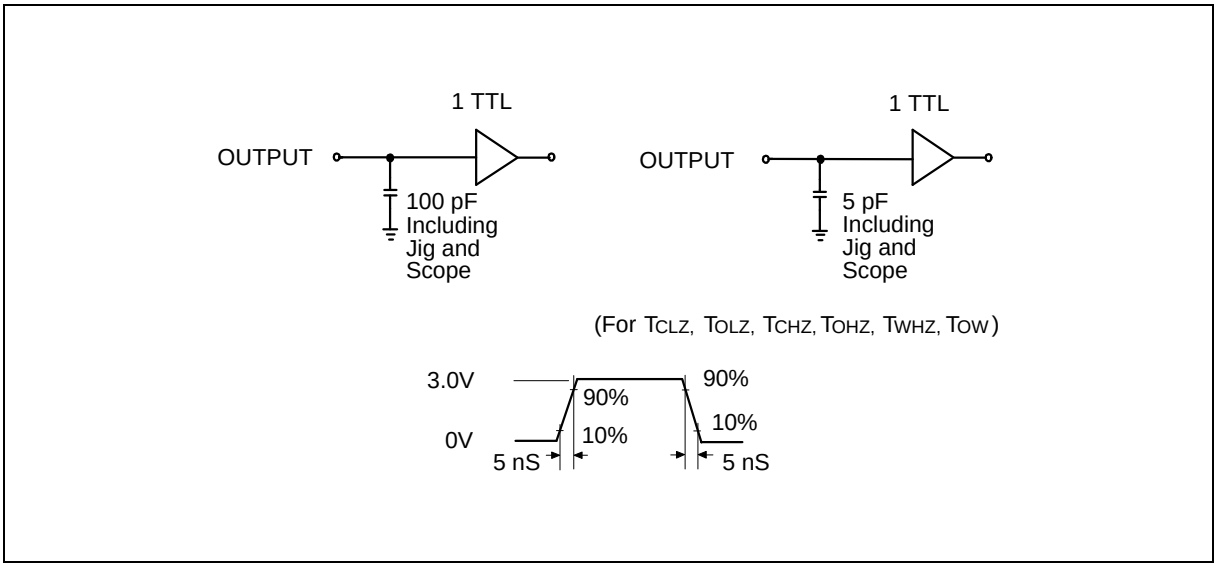
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	See the drawing below

AC Test Loads and Waveform



AC Characteristics, continued

(V_{DD} = 5V ±10%; V_{SS} = 0V; T_A (°C) = 0 to 70 for LL, -20 to 85 for LE)

Read Cycle

PARAMETER	SYM.	W24100-70L		W24100-70LL/LE		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T_{RC}	70	-	70	-	nS
Address Access Time	T_{AA}	-	70	-	70	nS
Chip Select Access Time	T_{ACS}	-	70	-	70	nS
Output Enable to Output Valid	T_{AOE}	-	35	-	35	nS
Chip Selection to Output in Low Z	T_{CLZ}*	10	-	10	-	nS
Output Enable to Output in Low Z	T_{OLZ}*	5	-	5	-	nS
Chip Deselection to Output in High Z	T_{CHZ}*	-	30	-	30	nS
Output Disable to Output in High Z	T_{OHZ}*	-	30	-	30	nS
Output Hold from Address Change	T_{OH}	10	-	10	-	nS

* These parameters are sampled but not 100% tested

Write Cycle

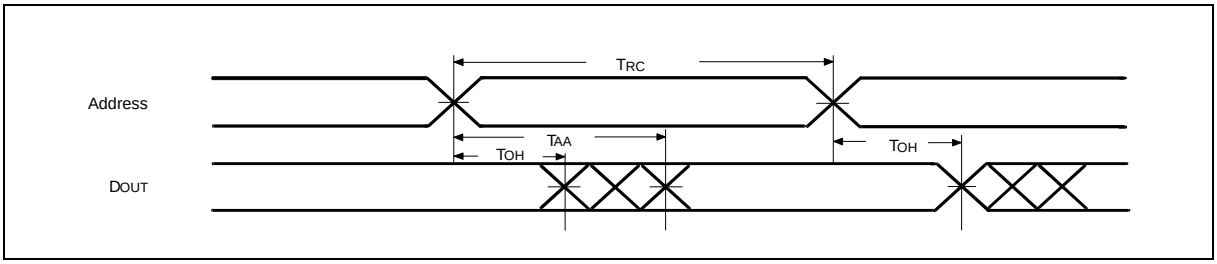
PARAMETER		SYM.	W24100-70L		W24100-70LL/LE		UNIT
			MIN.	MAX.	MIN.	MAX.	
Write Cycle Time		T_{WC}	70	-	70	-	nS
Chip Selection to End of Write		T_{CW}	50	-	50	-	nS
Address Valid to End of Write		T_{AW}	50	-	50	-	nS
Address Setup Time		T_{AS}	0	-	0	-	nS
Write Pulse Width		T_{WP}	50	-	50	-	nS
Write Recovery Time	#CS1, CS2, #WE	T_{WR}	0	-	0	-	nS
Data Valid to End of Write		T_{DW}	30	-	30	-	nS
Data Hold from End of Write		T_{DH}	0	-	0	-	nS
Write to Output in High Z		T_{WHZ}*	-	25	-	25	nS
Output Disable to Output in High Z		T_{OHZ}*	-	25	-	25	nS
Output Active from End of Write		T_{OW}	5	-	5	-	nS

* These parameters are sampled but not 100% tested

TIMING WAVEFORMS

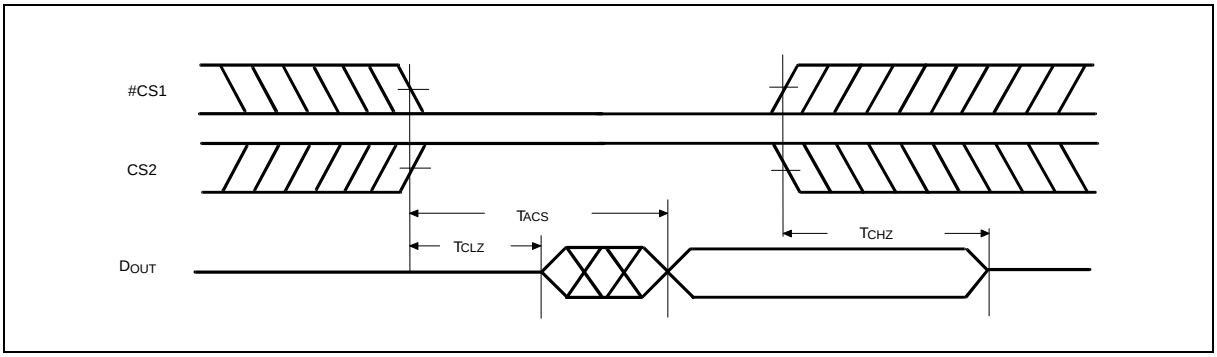
Read Cycle 1

(Address Controlled)



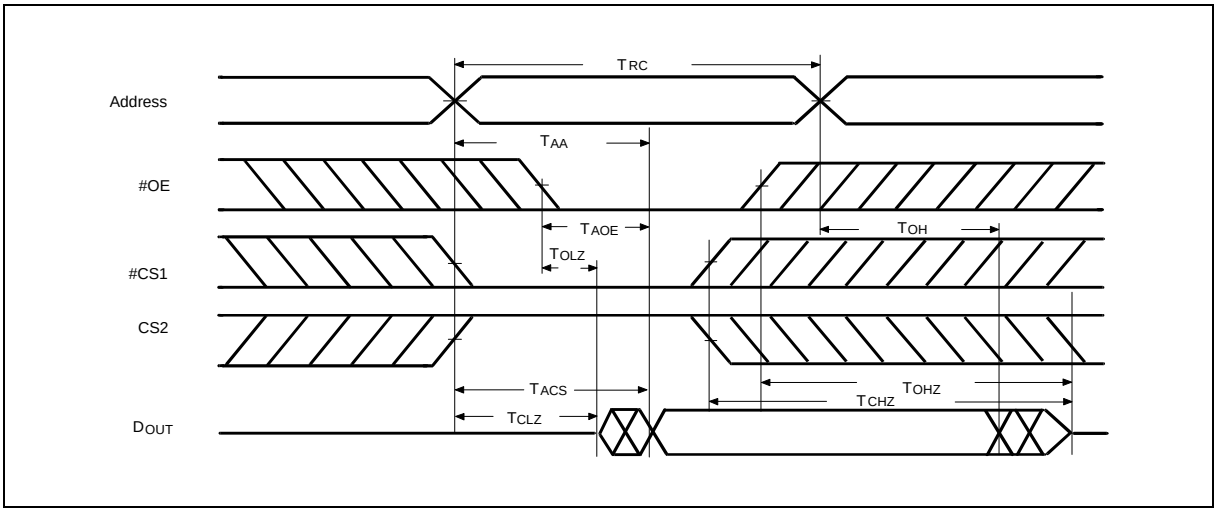
Read Cycle 2

(Chip Select Controlled)



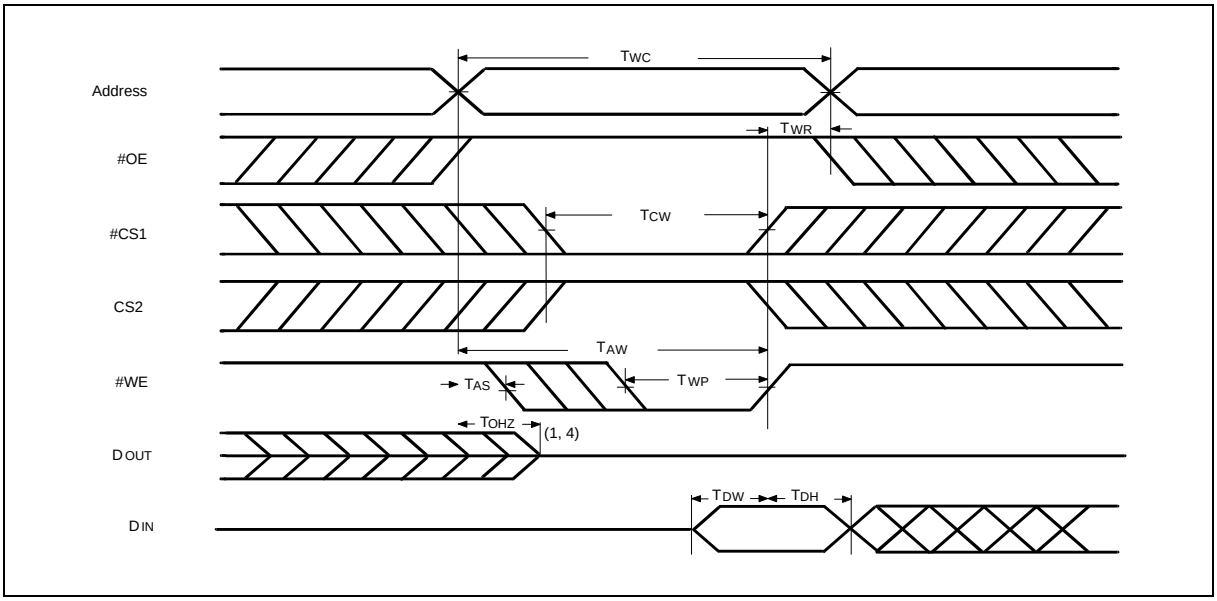
Read Cycle 3

(Output Enable Controlled)



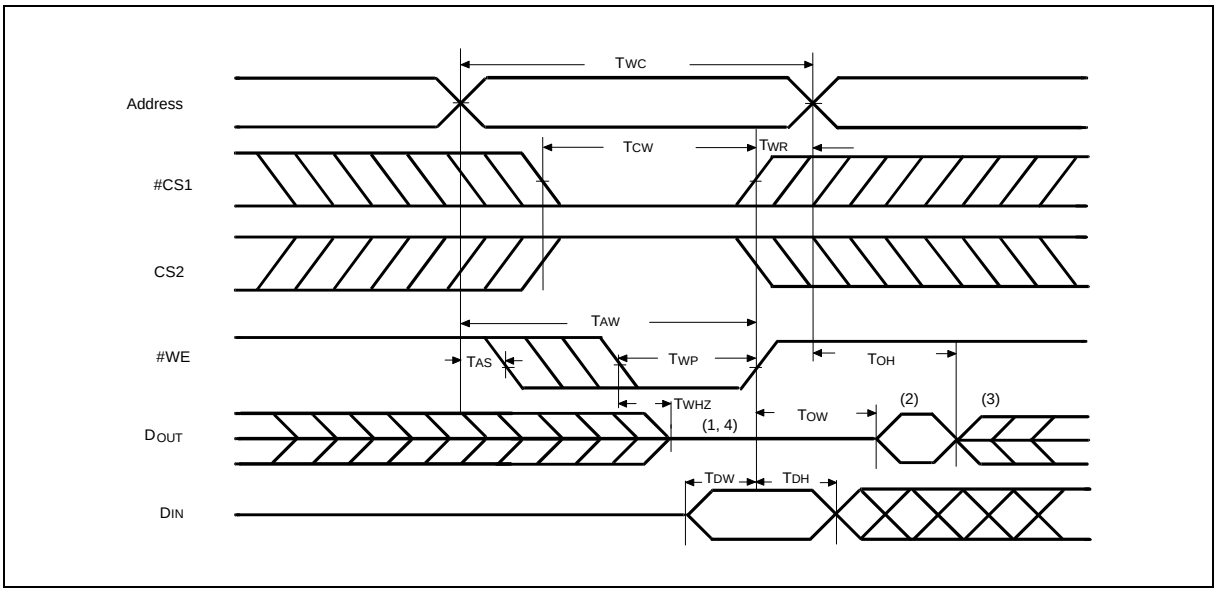
Timing Waveforms, continued

Write Cycle 1



Write Cycle 2

(#OE = VIL Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ±500 mV from steady state with CL = 5 pF. This parameter is guaranteed but not 100% tested.

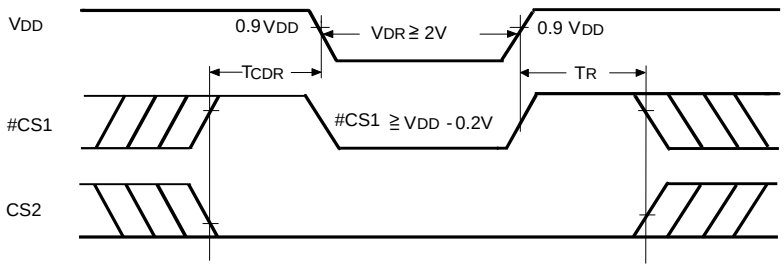
DATA RETENTION CHARACTERISTICS

(T_A (°C) = 0 to 70 for LL, -20 to 85 for LE)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD} for Data Retention	V_{DR}	#CS1 ≥ V_{DD} -0.2V	2.0	-	-	V
Data Retention Current	I_{DDDR}	#CS1 ≥ V_{DD} -0.2V, V_{DD} = 3V	-	-	50	µA
Chip Deselect to Data Retention Time	T_{CDR}	See data retention waveform	0	-	-	nS
Operation Recovery Time	T_R		T_{RC}*	-	-	nS

* Read Cycle Time

DATA RETENTION WAVEFORM



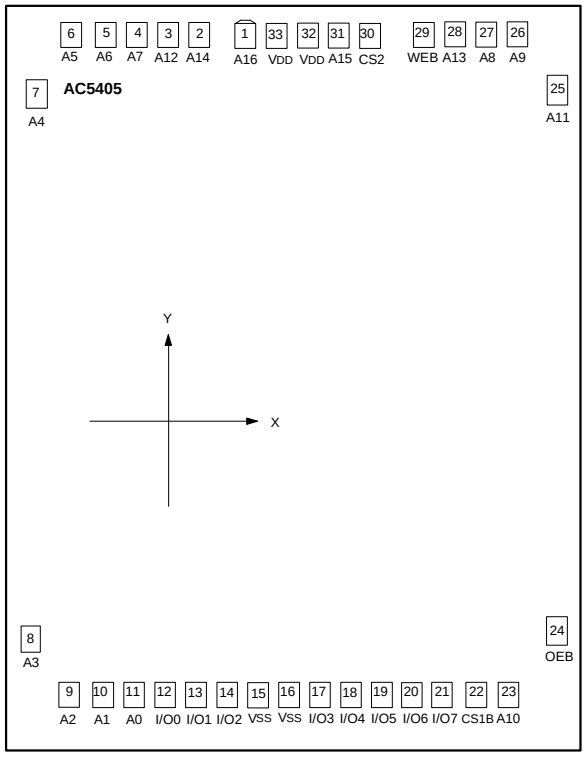
ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (μA)	PACKAGE
W24100-70L	70	70	100	600 mil DIP
W24100-70LL	70	70	50	600 mil DIP
W24100-70LE	70	70	70	600 mil DIP
W24100S-70L	70	70	100	450 mil SOP
W24100S-70LL	70	70	50	450 mil SOP
W24100S-70LE	70	70	70	450 mil SOP
W24100T-70L	70	70	100	Standard type one TSOP
W24100T-70LL	70	70	50	Standard type one TSOP
W24100T-70LE	70	70	70	Standard type one TSOP
W24100Q-70L	70	70	100	Small type one TSOP
W24100Q-70LL	70	70	50	Small type one TSOP
W24100Q-70LE	70	70	70	Small type one TSOP

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

BONDING PAD DIAGRAM



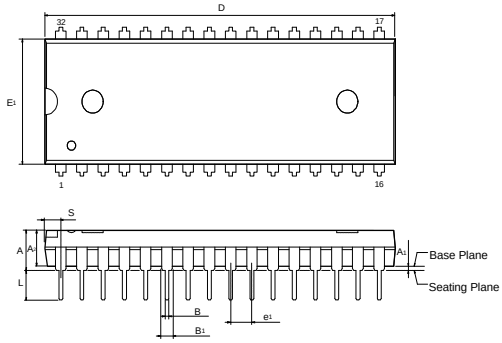
PAD NO.	X	Y
1	-485.31	2376.64
2	-1200.87	2376.64
3	-1341.05	2376.64
4	-1480.80	2376.64
5	-1622.21	2376.64
6	-1767.47	2376.64
7	-1993.03	2228.49
8	-1990.55	-2275.79
9	-1789.57	-2382.05
10	-1556.20	-2382.05
11	-1405.83	-2382.05
12	-1169.73	-2383.00
13	-870.28	-2383.00
14	-567.65	-2383.00
15	-336.94	-2385.00
16	-112.55	-2385.00
17	224.85	-2383.00
18	497.55	-2383.00
19	772.25	-2383.00
20	1044.95	-2383.00
21	1319.65	-2383.00
22	1537.77	-2382.05
23	1773.94	-2382.05
24	1985.78	-2297.62
25	1987.47	2221.27
26	1669.63	2376.64
27	1451.03	2376.64
28	1196.59	2376.64
29	956.65	2376.64
30	219.67	2376.64
31	79.47	2376.64
32	-145.06	2343.58
33	-353.56	2343.58

Note: For bare chip form (C.O.B.) applications, the substrate must be connected to V_{DD} or left floating in the PCB layout.

Winbond Electronics Corp.

PACKAGE DIMENSIONS

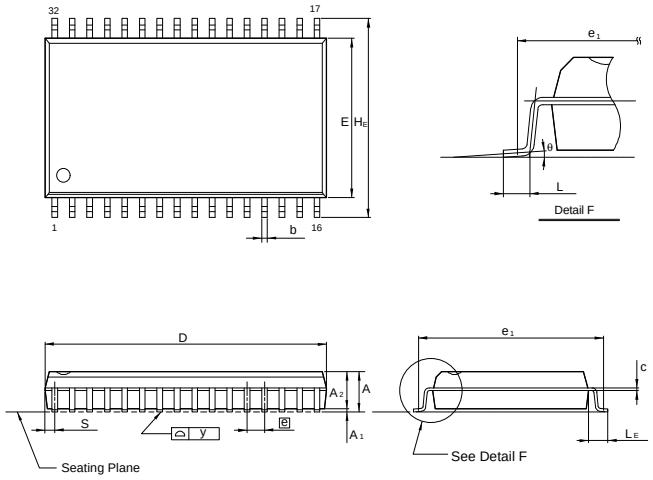
32-pin P-DIP



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.048	0.050	0.054	1.22	1.27	1.37
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.650	1.660	—	41.91	42.16
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.545	0.550	0.555	13.84	13.97	14.10
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.085	—	—	2.16

Notes:
1. Dimensions D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash
3. Dimensions D & E1 include mold mismatch ar are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches
6. General appearance spec. should be based o final visual inspection spec.

32-pin SOP Wide Body

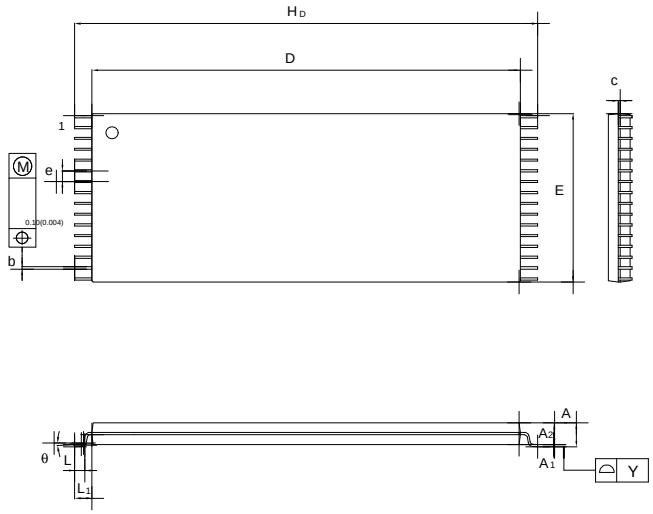


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.118	—	—	3.00
A_1	0.004	—	—	0.10	—	—
A_2	0.101	0.106	0.111	2.57	2.69	2.82
b	0.014	0.016	0.020	0.36	0.41	0.51
c	0.006	0.008	0.012	0.15	0.20	0.31
D	—	0.805	0.817	—	20.45	20.75
E	0.440	0.445	0.450	11.18	11.30	11.43
e	0.044	0.050	0.056	1.12	1.27	1.42
H_E	0.546	0.556	0.556	13.87	14.12	14.38
L	0.023	0.031	0.039	0.58	0.79	0.99
L_E	0.047	0.055	0.063	1.19	1.40	1.60
S	—	—	0.036	—	—	0.91
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

Notes:
1. Dimensions D Max. & S include mold flash or tie bar burrs.
2. Dimension b does not include dambar protrusion/intrusion.
3. Dimensions D & E include mold mismatch and determined at the mold parting line.
4. Controlling dimension: Inches
5. General appearance spec should be based on final visual inspection spec.

Package Dimensions, continued

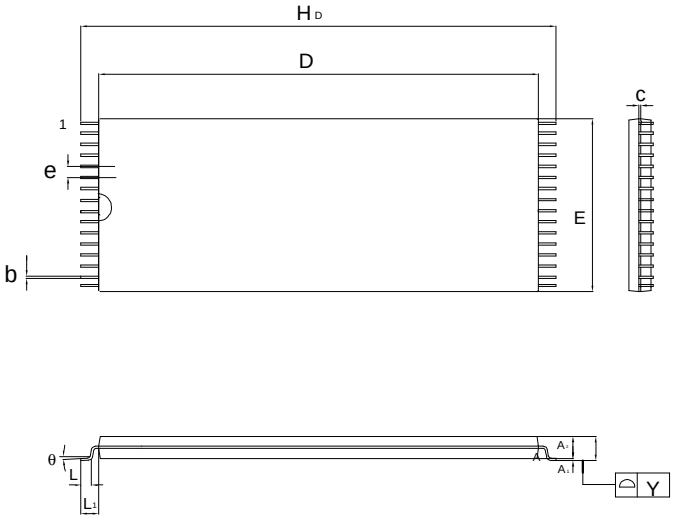
32-pin Standard Type One TSOP



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.047	—	—	1.20
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.008	0.009	0.17	0.20	0.23
c	0.005	0.006	0.007	0.12	0.15	0.17
D	0.720	0.724	0.728	18.30	18.40	18.50
E	0.311	0.315	0.319	7.90	8.00	8.10
H_D	0.780	0.787	0.795	19.80	20.00	20.20
e	—	0.020	—	—	0.50	—
L	0.016	0.020	0.024	0.40	0.50	0.60
L_1	—	0.031	—	—	0.80	—
Y	0.000	—	0.004	0.00	—	0.10
θ	1	3	5	1	3	5

Controlling dimension: Millimeters

32-pin Small Type One TSOP



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.049	—	—	1.25
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.008	0.009	0.17	0.20	0.27
c	0.0056	0.0059	0.0062	0.14	0.15	0.16
D	0.461	0.465	0.469	11.70	11.80	11.90
E	0.311	0.315	0.319	7.90	8.00	8.10
H_D	0.520	0.528	0.536	13.20	13.40	13.60
e	—	0.020	—	—	0.50	—
L	0.012	0.020	0.028	0.30	0.50	0.70
L_1	0.027	—	—	0.675	—	—
Y	0.000	—	0.004	0.00	—	0.10
θ	0	3	5	0	3	5

Controlling dimension: Millimeters

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Oct. 1999	-	Initial Issued
A2	May 2000	1, 2, 7, 8, 9	Add LE in Operating Characteristics, Data Retention Characteristics, Ordering Info; & Delete 32-pin P-DIP Package.
		9	Add in Bonding Pad Diagram
		2, 8	Standby Current for LE is 70 µA
A3	Sep. 6, 2001	1, 8, 10	Add in 32-pin P-DIP Package

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