

FEATURES

- Evaluation board is designed to be used together with accompanying software to implement a fully functional energy meter (watt-hour meter)**
- Easy connection of various external transducers via screw terminals**
- Easy modification of signal conditioning components using PCB sockets**
- LED indicators on logic outputs CF, ZX, SAG, and IRQ**
- Optically isolated data output connection to PC parallel port**
- Optically isolated frequency output (CF) to BNC**
- External reference option available for on-chip reference evaluation**

GENERAL DESCRIPTION

The ADE7763 is a high accuracy electrical power measurement IC with a serial interface and pulse output. The ADE7763 incorporates two second-order Σ - Δ ADCs, reference circuitry, temperature sensor, and all the signal processing required to perform active and apparent energy measurement.

This data sheet describes the ADE7763 evaluation kit's hardware and software functionality. The ADE7763 evaluation board, together with the ADE7763 data sheet and the EVAL-ADE7763EB data sheet, provides a complete evaluation platform for the ADE7763.

The evaluation board was designed so that the ADE7763 can be evaluated in the end application, i.e., watt-hour meter. Using the appropriate transducers on the current channel, e.g., di/dt sensor, CT, and shunt, the evaluation board can be connected to a test bench or high voltage (240 V rms) test circuit. An on-board resistor divider network provides the attenuation for the line voltage. This data sheet also describes how the current transducers should be connected for the best performance. The ADE7763 has a built-in digital integrator that allows for simple interfacing with any di/dt sensor (such as the Rogowski coil).

The evaluation board (watt-hour meter) is configured and calibrated via the parallel port of a PC. The data interface between the evaluation board and the PC is fully isolated. Windows® based software is provided with the evaluation board so it can be configured quickly as an energy meter.

The evaluation board also functions as a standalone evaluation system, which can be incorporated easily into an existing system via a 25-way D-Sub connector.

The evaluation board requires two external 5 V power supplies (one is required for isolation purposes) and the appropriate current transducer.

FUNCTIONAL BLOCK DIAGRAM

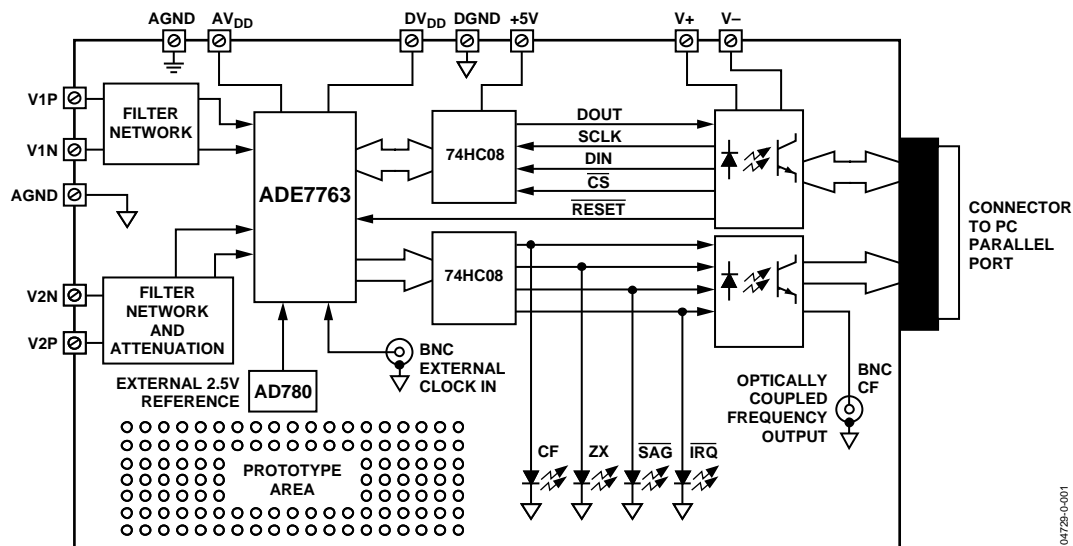


Figure 1.

04725-0-001

Rev. 0

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REVISION HISTORY

4/04—Revision 0: Initial Version

ANALOG INPUTS (SK1 AND SK2)

Voltage and current signals are connected at the screw terminals SK1 and SK2, respectively. All analog input signals are filtered using the on-board antialiasing filters before being presented to the analog inputs of the ADE7763. The default component values, which are shipped with the evaluation board, are the recommended values for the ADE7763. Users can easily change these components if they are familiar with selecting the component values for the analog input filters. Interested users are encouraged to refer to the [ADE7763](#) data sheet for a more comprehensive description of the antialiasing filters and their function.

CURRENT SENSE INPUTS (SK2)

SK2 is a 3-way connection block that allows the ADE7763 to be connected to a current transducer. Figure 2 shows the connector SK2 and the filtering network provided on the evaluation board.

The resistors SH1A and SH1B are by default not populated. They should be used as burden resistors when a CT is used as the current transducer (see the Using a CT as the Current Transducer section).

The RC networks R41/C11 and R42/C21 provide attenuation of high frequency noise and equalize the 20 dB/dec gain at high frequency when the di/dt sensor is used as the current transducer (see the Using a di/dt Sensor as the Current Transducer section). These RC networks are easily disabled by placing JP15 and JP25 and removing C11 and C21 (socketed).

The RC networks are the antialiasing filters required by the on-chip ADCs. The default corner frequency for these low-pass filters (LPF) is selected as 4.8 kHz (1 kΩ and 33nF). These filters can easily be adjusted by replacing the components on the evaluation board.

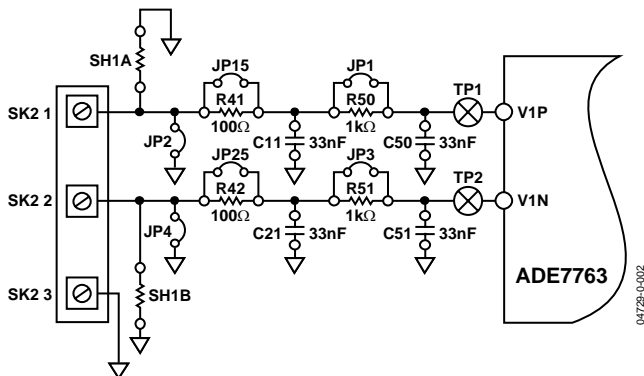


Figure 2. Current Channel on the ADE7763 Evaluation Board

USING A DI/DT SENSOR AS THE CURRENT TRANSDUCER

Figure 3 shows how a di/dt sensor can be used as a current transducer in a signal-phase, 2-wire distribution system. A di/dt sensor is typically made from an air-core coil. Because of the mutual inductance between the coil and the phase wire, a voltage signal is output from the coil, which is proportional to the time differentiation of the current (di/dt).

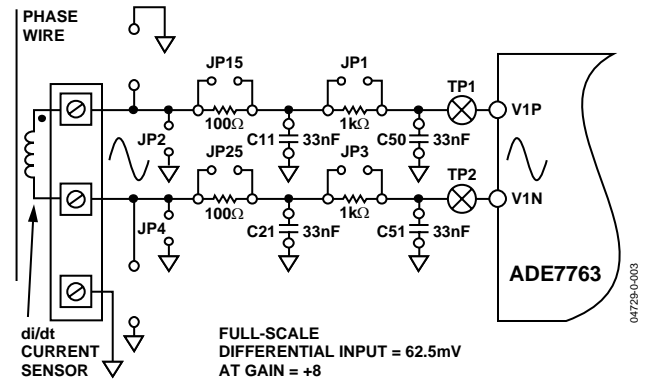


Figure 3. di/dt Sensor Connection to Current Channel

The di/dt sensor outputs a voltage by mutual inductance. When using a di/dt sensor as the current sensor, Jumpers JP15/JP25 and JP1/JP3 should be left open. Both sets of filters are necessary to provide the antialiasing filters (see Figure 3).

In theory, air-core di/dt sensors have an associated phase shift of +90° at all input frequencies. This phase shift is compensated by the -90° phase shift of the integrator. Additional phase error, from external component mismatch, for example, can be corrected by writing to the phase calibration register (PHCAL[7:0]) in the ADE7763. The software supplied with the ADE7763 evaluation board allows users to adjust the phase calibration register. See the Evaluation Software section for more information.

For this example, notice that the maximum analog input range on Channel 1 is set to 62.5 mV, and the gain for Channel 1 has been set to 8. The maximum analog input range and gain are set via the gain register (GAIN). See the [ADE7763](#) data sheet. The evaluation software allows users to configure the channel range and gain. The maximum peak differential signal on Channel 1 is 0.5 V (at Gain = +1).

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USING A CT AS THE CURRENT TRANSDUCER

Figure 4 shows how a CT can be used as a current transducer in a signal-phase, 3-wire distribution system. This is how electrical energy is distributed to residential users in the United States. Phase A and Phase B are nominally 180° out of phase. The vector addition of the two currents is easily achieved by using two primary turns of opposite polarity on the CT.

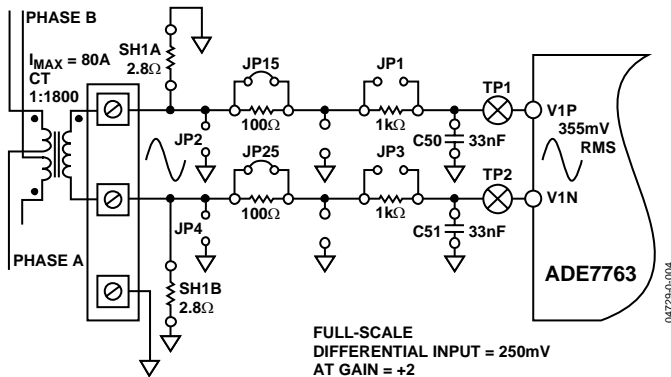


Figure 4. CT Connection to Current Channel

The CT secondary current is converted to a voltage by using a burden resistance across the secondary winding outputs. Care should be taken when using a CT as the current transducer. If the secondary is left open, i.e., no burden is connected, a large voltage could be present at the secondary outputs. This can cause an electrical shock hazard and potentially damage electronic components.

When using a CT as the current sensor, the phase compensation network for a shunt application should be disabled. This is achieved by closing Jumpers JP15/JP25 and removing C11/C21.

The antialiasing filters should be enabled by opening Jumpers JP1/JP3 (see Figure 4).

Most CTs have an associated phase shift of between 0.1° and 1° at 50 Hz/60 Hz. This phase shift or phase error can lead to significant energy measurement errors, especially at low power factors. However, this phase error can be corrected by writing to the phase calibration register (PHCAL[7:0]) in the ADE7763. The software supplied with the ADE7763 evaluation board allows users to adjust the phase calibration register. See the Evaluation Software section for more information.

For this example, notice that the maximum analog input range on Channel 1 is set to 250 mV, and the gain for Channel 1 has been set to 2. The maximum analog input range and gain are set via the gain register (GAIN). See the ADE7763 data sheet. The evaluation software allows users to configure the channel range and gain.

USING A SHUNT RESISTOR AS THE CURRENT TRANSDUCER

Figure 5 shows how a shunt resistor can be used to perform the current-to-voltage conversion required for the ADE7763. A shunt is a cost-effective way to perform the current-to-voltage conversion in a 2-wire, single-phase application. No isolation is required in a 2-wire application, and the shunt has advantages over the CT arrangement. For example, a shunt does not suffer from dc saturation problems, and the phase response of the shunt is linear over a very wide dynamic range. Although the shunt is predominately resistive, it does have parasitic reactive elements (inductance) that can become significant, even at 50 Hz/60 Hz. This means that there can be a small phase shift associated with the shunt. Once it is understood, the phase shift is easily compensated for with the filter network R41/C11 and R42/C21 (see Application Note AN-559 for more details).

The shunt used in this example is a 200 μΩ Manganin® type. The resistance of the shunt should be as low as possible in order to avoid excessive power dissipation in the shunt. Figure 5 shows how the shunt can be connected to the evaluation board. Two sense wires should be soldered to the shunt as shown at the copper/Manganin junctions. These sense wires should be formed into a twisted pair to reduce the loop area that reduces antenna effects. A connection for the common-mode voltage can be made at the connection point for the current-carrying conductor (see Figure 5).

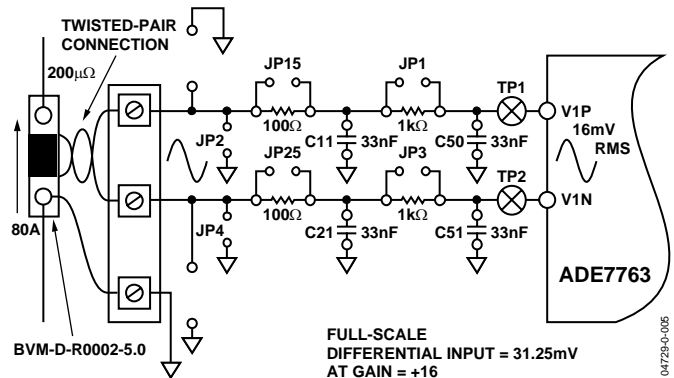


Figure 5. Shunt Connection to Current Channel

VOLTAGE SENSE INPUTS

The voltage input connections on the ADE7763 evaluation board can be directly connected to the line voltage source.

The line voltage is attenuated using a simple resistor divider network before it is presented to the ADE7763. Because of the relatively large signal on this channel and the small dynamic range requirement, the voltage channel can be configured in a single-ended configuration. Figure 6 shows a typical connection for the line voltage.

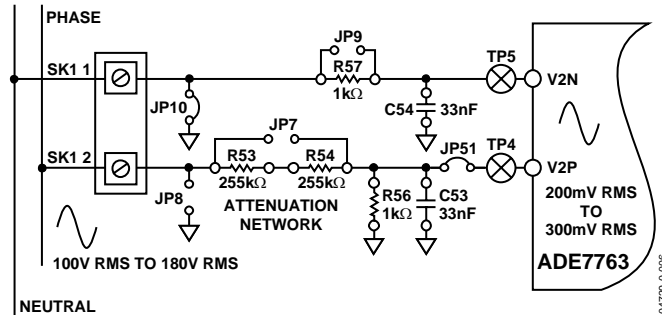


Figure 6. Voltage Channel on the ADE7763 Evaluation Board

Note that the analog input V2N is connected to AGND via the antialiasing filter R57/C54 using JP10. Also, Jumper JP9 should be left open.

The voltage attenuation network is made up of R53, R54, and R56. The maximum signal level permissible at V2P is 0.5 V peak. Although the ADE7763 analog inputs can withstand ± 6 V without risk of permanent damage, the signal range should not exceed ± 0.5 V with respect to AGND for specified operation.

The attenuation network can be easily modified by the user to accommodate any input signal levels. However, the value of R56 (1 k Ω) should not be altered as the phase response of Channel 2 should match the phase response of Channel 1 (see Application Note [AN-559](#)).

JUMPER SETTINGS

Table 1.

Jumper	Option	Description
JP1	Closed	This shorts out R50. The effect is to disable the antialiasing filter on the analog input V1P. Default open.
	Open	Enable the antialiasing filter on V1P.
JP2	Closed	This connects the analog input V1P to ground. Default open.
JP3	Closed	This shorts out R51. The effect is to disable the antialiasing filter on the analog input V1N. Default open.
	Open	Enable the antialiasing filter on V1N.
JP4	Closed	This connects the analog input V1N to ground. Default open.
JP5	A	This connects the buffered logic output \overline{IRQ} to the LED1.
	B	This connects the buffered logic output \overline{IRQ} to Pin 10 on the D-Sub connector via an optical isolator.
JP6	A	This connects the buffered logic output \overline{SAG} to the LED2.
	B	This connects the buffered logic output \overline{SAG} to Pin 11 on the D-Sub connector via an optical isolator.
JP7	Closed	This shorts the attenuation network on Channel 2. Default open.
JP8	Closed	This connects the analog input V2P to ground. Default open.
JP9	Closed	This shorts out R57. The effect is to disable the antialiasing filter on the analog input V2N. Default open.
	Open	Enable the antialiasing filter on V2N.
JP10	Closed	This connects the analog input V2N to ground. Default open.
JP11	Closed	This connects the analog and digital ground planes of the PCB. Default closed.
JP12	A	This connects the buffered logic output CF to the LED4.
	B	This connects the buffered logic output CF to the BNC2 connector via an optical isolator.
JP13	Closed	This connects an external reference 2.5 V (AD780) to the ADE7763.
	Open	This enables the ADE7763 on-chip reference.
JP14	Closed	This connects the optical isolator ground to the evaluation board ground (DGND). If full isolation between the evaluation board and PC is required, this jumper should be left open.
	Open	This connects the optical isolator ground to the evaluation board ground (DGND). If full isolation between the evaluation board and PC is required, this jumper should be left open.
JP15	Closed	This shorts out R41. The effect is to disable the first-state antialiasing filter (for di/dt sensors or for shunts) on the analog input V1P. Default open.
	Open	Enable the antialiasing filter on V1P.
JP19	A	This connects the buffered logic output ZX to the LED3.
	B	This connects the buffered logic output ZX to Pin 12 on the D-Sub connector via an optical isolator.
JP20	Closed	This connects the AVDD and DVDD supply for the evaluation board together. Default closed.
JP21	Closed	This connects the DVDD and 5 V (buffers) supply for the evaluation board together. Default closed.
JP25	Closed	This shorts out R42. The effect is to disable the first-state antialiasing filter (for di/dt sensors or shunt) on the analog input V1N. Default open.
JP51	Closed	This shorts out/disconnects analog input V2P from the ADE7763. Default closed.

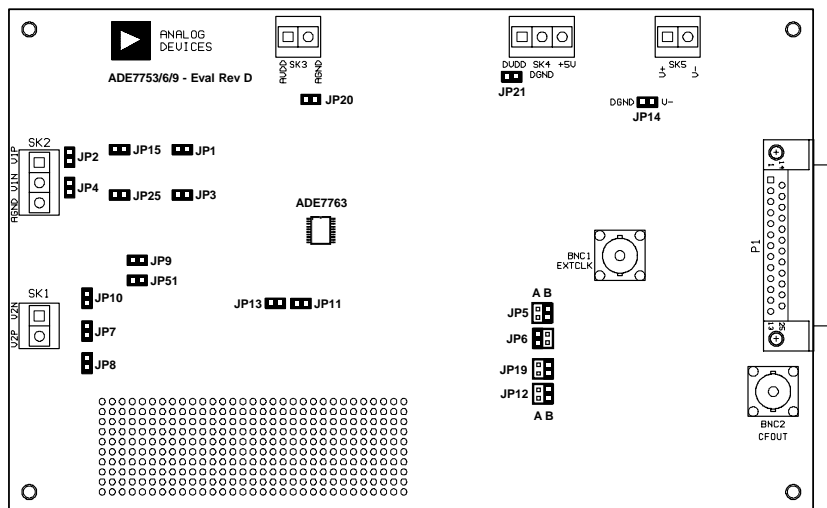


Figure 7. ADE7763 Evaluation Board Jumper Positions

SETTING UP THE ADE7763 EVALUATION BOARD

Figure 8 shows a typical setup for the ADE7763 evaluation board. In this example, a kWh meter for a 2-wire, single-phase distribution system is shown. For a more detailed description on how to use a di/dt as a current transducer, see the Current Sense Inputs (SK2) section. The line voltage is connected directly to the evaluation board, as shown in Figure 8. Note JP7 should be left open to ensure that the attenuation network is not bypassed, and also note the use of two power supplies. The second power supply is used to power the optical isolation. With JP14 left open, there is no electrical connection between the high voltage test circuit and the PC. The power supplies should have floating voltage outputs.

The evaluation board is connected to the PC parallel port using the cable supplied. The cable length should not exceed 6 feet (2 meters) or the serial communication between the PC and the evaluation board may become unpredictable and error prone.

When the evaluation board has been powered up and is connected to the PC, the supplied software can be launched. The software automatically starts in energy meter mode. The next section describes how the ADE7763 evaluation software can be installed and removed.

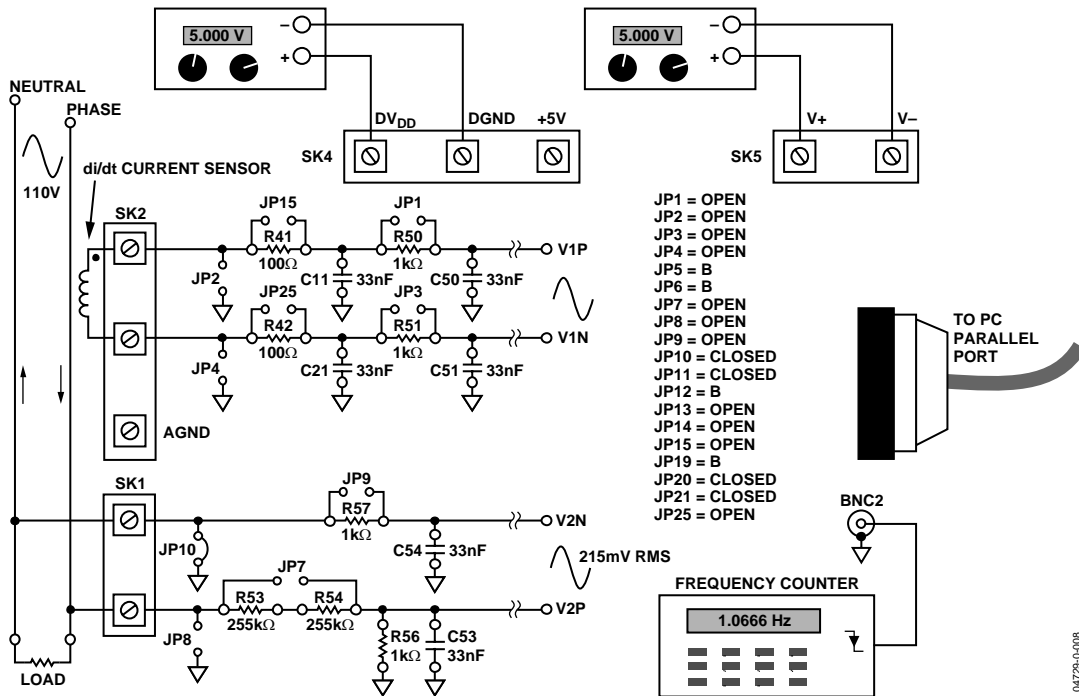


Figure 8. Typical Setup for the ADE7763 Evaluation Board

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EVALUATION SOFTWARE

The ADE7763 evaluation board is supported by Windows based software that allows users to access all the functionality of the ADE7763. The software is designed to communicate with the ADE7763 evaluation board via the parallel port of the PC.

INSTALLING THE ADE7763 SOFTWARE

The ADE7763 software is supplied on a CD. The minimum requirements for the PC are Pentium® II 233 MHz processor, 32 MB RAM, 10 MB free HD space, and at least one PS/2 or ECP parallel port. To install the software place the CD in the drive and double-click setup.exe. This launches the setup program, which automatically installs all the software components, including the uninstall program, and creates the required directories. When the setup program has finished installing the ADE7763eval program, users are prompted to install National Instruments' run-time engine. This software was developed using National Instruments' LabVIEW™ software, and the run-time engine is required to run the ADE7763eval program. GIVEIO software is required to run the program on all systems. Users are prompted to install this software as well, and they should follow the on-screen instructions to complete the installation. Users need to reboot their computers to complete the installation. To launch the software, select Start—>Programs—>ADE7763 menu and click ADE7763eval.

REMOVING THE ADE7763 EVALUATION SOFTWARE

The ADE7763Eval program, National Instruments' run-time engine, and GIVEIO are easily removed by using the Add or Remove Programs feature in the Control Panel. Select Start—>Control Panel—>Add or Remove Programs and click the program to remove it.

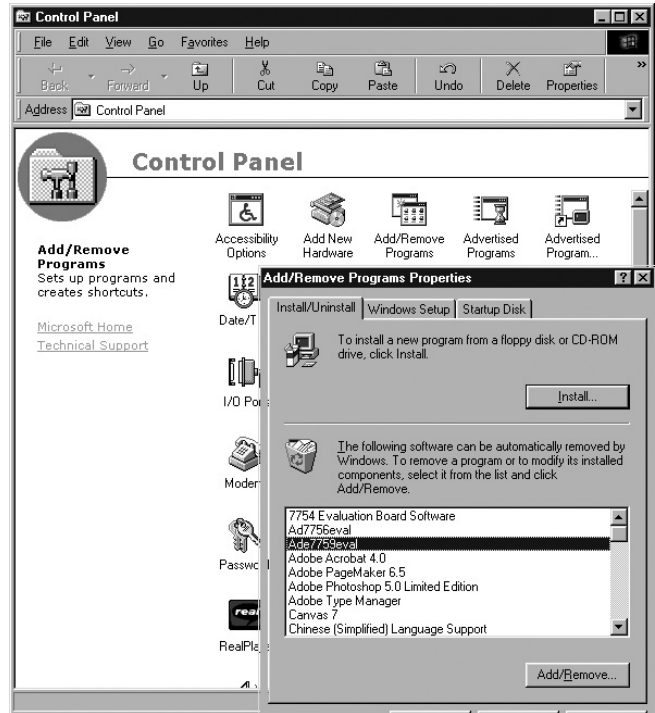


Figure 9. Removing the ADE7763 Evaluation Software

MAIN MENU

When the software is launched, the program automatically displays the main menu shown in Figure 10. To stop the ADE7763eval software, select Exit from the menu. Each of the 9 selections in the menu starts a new window that accesses the registers and displays information from the ADE7763. By pressing the Exit button in the new window, users are brought back to the main menu. Register values are not reset by the program when a new window opens or closes. The register addresses and functionality can be found in the [ADE7763 data sheet](#).

Using the ADE7763eval software, the evaluation board can be used as a fully functional energy meter. When the appropriate line voltage, test current, frequency, and meter constant are set up, users can use the calibration routine to remove any errors associated with the transducers. The CF output can be used with a standard frequency counter to check the accuracy. The measured CF output frequency should be adjusted to match the theoretical CF frequency of the evaluation software.

Note that the calibration routine does not automatically remove the phase mismatch errors associated with the current and voltage transducer. These must be removed by using the ADE7763 PHCAL register. This is explained in the Measuring CT Phase Errors Using the ADE7763 section. The calibration routine is launched by selecting Calibration from the menu.

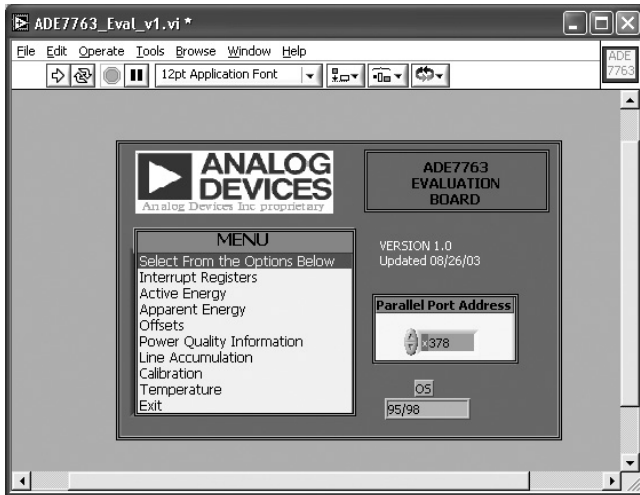


Figure 10. Main Menu

Note also that the input signal range and gain must be set for the PGAs on Channel 1 and Channel 2. This ensures that the output signal range from the transducers is matched to the analog inputs. For example, by selecting a gain of 1 for the PGA in Channel 2, the peak differential input signal is set to 500 mV. In the meter example shown in Figure 8, the line voltage is attenuated to approximately 215 mV rms or 304 mV peak. Similarly, as an example for Channel 1, assuming a maximum current of 120 A, the maximum differential output signal from the di/dt sensor is 30 mV rms or 42 mV peak (the value depends on the sensor used). To allow for surge current, the full-scale differential input signal level is set to 62 mV by setting the gain to 2 if the ADC input range is set to 0.125 V (see Table I in the ADE7763 data sheet). Access to the PGAs is allowed in the active energy and apparent energy windows that can be opened from the menu.

CALIBRATING THE METER

In order to calibrate the energy meter, the line voltage, test current, line frequency, and meter constant must be entered, as shown in Figure 11. In this example, the line voltage is 220 V, the test current is 5 A, the frequency is 50 Hz, and the required meter constant is 3,200 imp/kWh. The menu lists the option for calibrating active or apparent energy. Once the parameters are entered, the voltage and current circuits are energized, and the energy is selected, click the Calibrate button. The software then executes the calibration routine and automatically starts to register energy.

Calibration can be done by changing the CFDEN, CFNUM, and WGAIN (or VAGAIN) registers, which is explained in the ADE7763 data sheet. The measured CF output frequency is then adjusted to match the theoretical CF frequency of the evaluation software. To write to CFNUM, CFDEN, and WGAIN for manual calibration, click Adjust Values. Calibration should be run before this is done to calculate the target frequency.

Ensure that the analog input signal levels have been matched to the transducer output signal levels, as previously described.

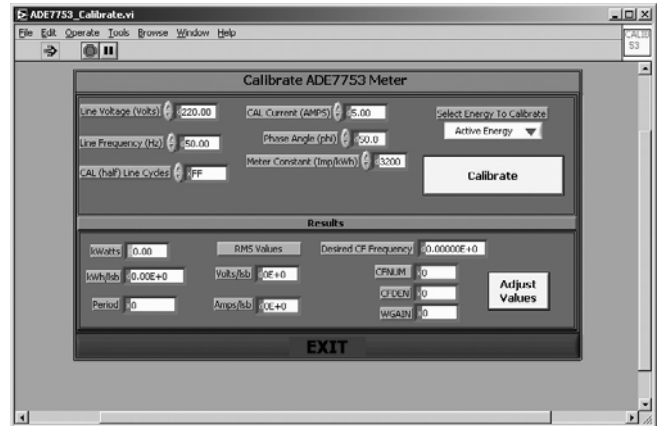


Figure 11. Calibration Window

MENU SELECTIONS

The menu selections include the following: Interrupt Registers, Active Energy, Apparent Energy, Offsets, Power Quality Information, Line Accumulation, Calibration, and Temperature.

The mask and status interrupt registers described in the ADE7763 data sheet are accessible from the Interrupt Registers window. In the Active Energy and Apparent Energy windows, users can view the datapath, configure or reset the part by writing to the necessary registers, and read the active or apparent energy registers.

In addition, Waveform Sampling is available from any of these selections. Figure 12 shows the Active Energy window.

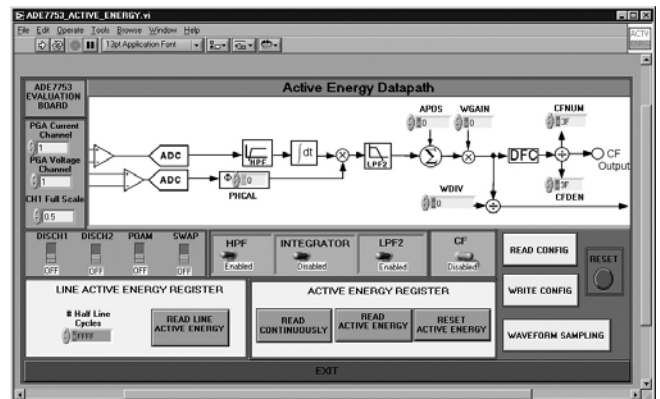


Figure 12. Active Energy Window

Channel 1, Channel 2, active power, and rms offset registers are accessible via the Offsets selection from the menu. The user may modify and view rms, peak, and SAG registers from the Power Quality window. Additionally, the relevant mask and status registers are presented in this window.

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The Line Accumulation window allows one to view line accumulation active energy and line accumulation apparent energy. To begin line accumulation, press the Start Read button. The number of line cycles can be changed in this window at any time.

WAVEFORM SAMPLING ROUTINE

In this mode, the evaluation software programs the ADE7763 for waveform sampling with an updated rate of 3.5 kSPS (CLKIN/1024). The user can define the number of samples needed and select the signal waveform to transfer. The options are Channel 1, Channel 2, or multiplier waveforms. Three parameters are processed when the waveform is displayed: rms value, mean value, and standard deviation. For comparison, the voltage and current rms registers are shown in the waveform sampling window (Figure 13). The waveform sampling routine can be accessed from the Active Energy, Apparent Energy, or Power Quality windows by pressing the Waveform Sampling button. Figure 13 shows the Waveform Sampling Window.

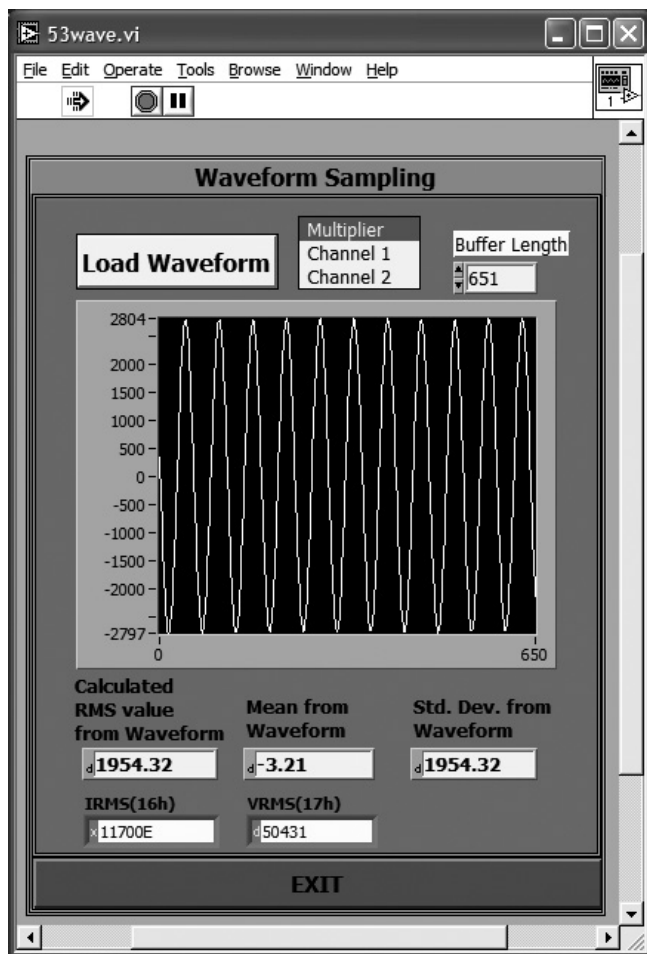


Figure 13. Waveform Sampling Window

When using this feature with sine wave signals, the user should be aware that if the samples represent a noninteger number of periods of the selected signal, then the rms and mean values are biased. To correct this, the number of samples should be chosen to give an integer number of signal cycles as follows:

$$\text{No. of Samples} = \frac{\text{No. of Signal Cycles} \times \text{ADE7763 CLKIN Frequency}}{1024 \times \text{Signal Frequency}}$$

ONLINE HELP

The ADE7763 evaluation software also comes with an online help feature. Select Help → Show Help on the menu (see Figure 14). A Help Window opens. For a description of a particular option, e.g., button or text box, move the cursor over the item. The Help window displays a description of the item.



Figure 14. Online Help Function

MEASURING CT PHASE ERRORS USING THE ADE7763

The ADE7763 can measure the phase error associated with the current sensor during calibration. The ADE7763 has negligible internal phase error (PHCAL = 00 hex), and the error due to external components is small (<0.5°). The procedure is based on a 2-point measurement, at PF = 1 and PF = 0.5 (lag). The PF is set up using the test bench source, and this source must be very accurate. The ADE7763 should be configured for energy measurement mode.

An energy measurement is first made with PF = 1 (Measurement A). A second energy measurement should be made at PF = 0.5 (Measurement B). The frequency output CF can be used for this measurement. Using the following formula, the phase error is easily calculated:

$$\text{Phase Error (}^\circ\text{)} = \tan^{-1}\left(\frac{B - A/2}{A/2 \times \sqrt{3}}\right)$$

For example, using the frequency output CF to measure power, a frequency of 3.66621 Hz is recorded for PF = 1. The PF is then set to 0.5 lag and a measurement of 1.83817 Hz is obtained. Using the formula above, the phase error on Channel 1 is calculated as:

$$\text{Phase Error (}^\circ\text{)} = \tan^{-1}\left(\frac{1.83817 - 3.66621/2}{3.66621/2 \times \sqrt{3}}\right) = 0.091^\circ$$

The formula also gives the correct sign for the phase error. In this example, the phase error is calculated as 0.091° at the input to Channel 1 of the ADE7763. This means that the current sensor has introduced a phase lead of 0.091°. Therefore, the phase difference at the input to Channel 1 is now 59.89° lag instead of 60° lag. Determining whether the error is a lead or lag can also be figured intuitively from the frequency output. Figure 15 shows how the output frequency varies with phase (cos {Φ}). Because the Output Frequency B (1.83817 Hz) at the PF = 0.5 lag setting in the example is actually greater than A/2 (1.833105 Hz), the phase error between Channel 1 and Channel 2 is actually less than 60°. This means there is additional lead in Channel 1 due to the CT.

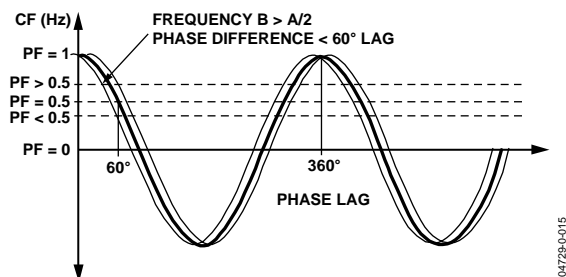


Figure 15. CF Frequency vs. Phase (PF)

USING PHASE CALIBRATION TO CORRECT SMALL (<0.5°) EXTERNAL PHASE ERRORS

From the previous example, it is seen that the CT introduced a phase lead in Channel 1 of 0.091°. Therefore, instead of a 60° phase difference between Channel 1 and Channel 2, it is actually 59.89°. In order to bring the phase difference back to 60°, the phase compensation circuit in Channel 2 is used to introduce an extra lead of 0.091°. This is achieved by reducing the amount of time delay in Channel 2.

The maximum time delay adjustment in Channel 2 is -97.86 μs to +39.96 μs with a CLKIN of 3.579545 MHz. The PHCAL register is a signed twos complement 6-bit register. Therefore, each LSB is equivalent to 2.22 μs. The default value of this register is 0x0D and is equivalent to 0.00°. In this example, the line frequency is 50 Hz. This means each LSB is equivalent to 360° × 2.22 μs × 50 Hz = 0.040°. To introduce a lead of 0.091°, the delay in Channel 2 must be reduced. This is achieved by writing 0xB or +0.08° to the PHCAL register. The PHCAL register can be written to by entering the value in the active energy window.

CORRECTING LARGE EXTERNAL PHASE ERRORS

In this example, the phase correction range at 50 Hz is approximately -1.76° to +0.7°. However, it is best to use the PHCAL register only for small phase corrections, i.e., <0.5°. If larger corrections are required, the larger part of the correction can be made using an external passive component. For example, the resistors in the antialiasing filter can be modified to shift the corner frequency of the filter to introduce more or less lag. The lag through the antialiasing filters with 1 kΩ and 33 nF is 0.56° at 50 Hz. Fine adjustment can be made with the PHCAL register. Note that typically CT phase shift does not vary significantly from part to part. If a CT phase shift is 1°, then the part-to-part variation should only be about ±0.1°. Therefore, the bulk of the phase shift (1°) can be canceled with fixed component values at design. The remaining small adjustments can be made in production using the PHCAL register.

EVALUATION BOARD BILL OF MATERIALS

Table 2.

Designator	Value	Description
R3, R5, R6, R13, R22, R30, R31, R33, R34, R37	100 Ω, 5%, ¼ Ω	Resistor, No Special Requirements.
R2, R7 to R10, R39, R40	10 kΩ, 5%, ¼ Ω	Resistor, No Special Requirements.
R1, R14 to R27, R36 R50 to R52, R57	820 Ω, 5%, ¼ Ω 1 kΩ, 0.1%, ¼ Ω	Resistor, No Special Requirements. ±5 ppm/°C Resistor, Good Tolerance, Used as Part of the Analog Filter Network. These resistors are not soldered but are plugged into the PCB pin sockets for easy modification by the customer. Low drift Vishay Dale Part No. CMF551001BT-2.
R53, R54	499 kΩ, 0.1%, ¼ Ω	±5 ppm/°C Resistor, Good Tolerance. Vishay Dale Part No. CMF554993FT-1.
R41, R42	100 Ω, 0.1%, ¼ Ω	±5 ppm/°C Resistor, Good Tolerance. Low drift Vishay Dale Part No. CMF551000BT-2.
R11	51 Ω, 1%, ¼ Ω	Not Populated, Pin Socket to Be Used with External 50 Ω Clock Source.
R4	0 Ω, 10%, ¼ Ω	
C5, C7, C24, C28, C30 C14, C15	10 μF, 10 V dc 22 pF, Ceramic	Power Supply Decoupling Capacitors, 20%, AVX-Kyocera, Farnell Part No. 643-579. Gate Oscillator Load Capacitors, Farnell Part No. 108-927.
C6, C8, C23, C25, C27, C29, C31 to C36	100 nF, 50 V	Power Supply Decoupling Capacitors, 10%, X7R type, AVX-Kyocera, Farnell Part No. 108-950.
C16	220 pF	AVX-Kyocera, Farnell Part No. 108-946.
C11, C21, C50, C51, C53, C54	33 nF, 10%, 50 V	X7R Capacitor, Part of the Filter Network. These resistors are not soldered but are plugged into the PCB mount sockets for easy modification by the customer. The SR15 series AVX-Kyocera, Farnell Part No. 108-948.
U1	ADE7763ARS	Supplied by Analog Devices, Inc.
U2, U3	74HC08	Quad CMOS AND Gates.
U4	AD780	2.5 V Reference, Supplied by Analog Devices, Inc.
U5, U7 to U9	HCPL2232	HP Optical Isolator, Newark Part No. 06F5434.
U6	HCPL2211	HP Optical Isolator, Newark Part No. 06F5428.
LED1 to LED4	LED	Low Current, Red, Farnell Part No. 637-087.
XTAL	3.579545 MHz	Quartz Crystal, HC-49 (US), ECS Part No. ECS-35-17-4. Digi-Key Part No. X079-ND.
SK1, SK3, SK5	Screw Terminal	15 A, 2.5 mm Cable Screw Terminal Sockets. Farnell Part No. 151-785, Length 10 mm, Pitch 5 mm, Pin Diameter 1 mm.
SK2, SK4	Screw Terminal	15 A, 2.5 mm Cable Screw Terminal Sockets. Farnell Part No. 151-786, Length 15 mm, Pitch 5 mm, Pin Diameter 1 mm.
BNC1, BNC2	BNC Connector	Straight Square, 1.3 mm Holes, 10.2 mm × 10.2 mm Farnell Part No. 149-453.
P1	D-Sub 25-Way Male	AMP 747238-4 Right Angle D-Sub 8 mm PCB Mount, Digi-Key Part No. 747238-4.
TP4 to TP14	Test Point Loop	Test Point Loop, Compnt Corp. TP-104-01-XX.
JP1 to JP4, JP7 to JP11, JP13 to JP15, JP20, JP21, JP25, JP51	2-Pin Header	2-Pin, 0.025 Sq., 0.01 Ctrs, Compnt Corp., CSS-02-02.
JP5, JP6, JP12, JP19	2-Pin Header × 2	2-Pin, 0.025 Sq., 0.01 Ctrs, Compnt Corp., CSS-02-02.
Pin Sockets	DIL	Sockets for U1 to U9, 0.022" to 0.025" Pin Diameter, ADI Stock 12-18-33. Advance KSS100-85TG.
Pin Sockets	Discretes	R11, R41, R42, R50 to R54, R57, C11, C21, C50 to C54. ADI Stock 12-18-41.

EVALUATION BOARD SCHEMATIC (REV. D AND REV. E)

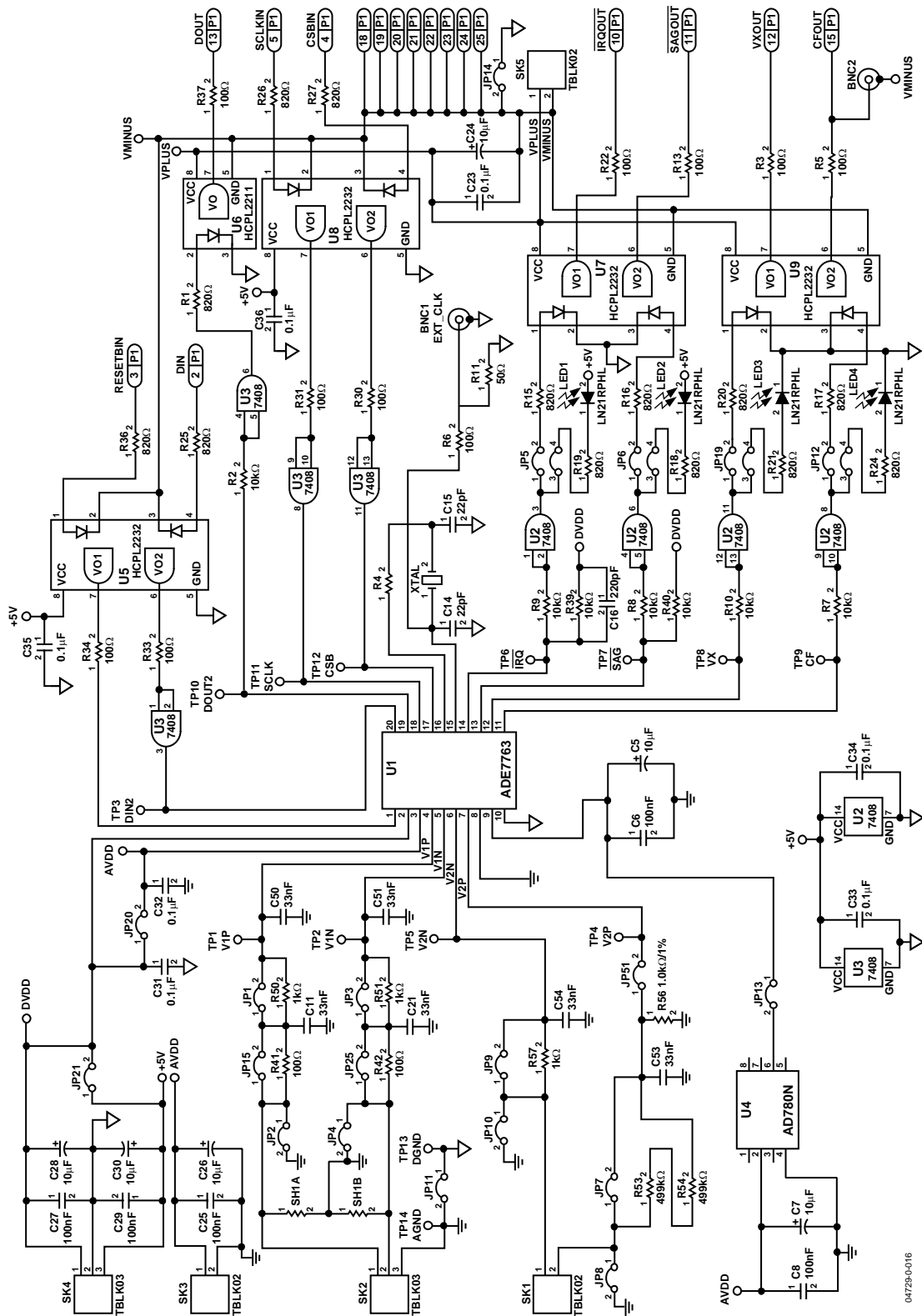


Figure 16. Evaluation Board Schematic

PCB LAYOUT—COMPONENT PLACEMENT (REV. D)

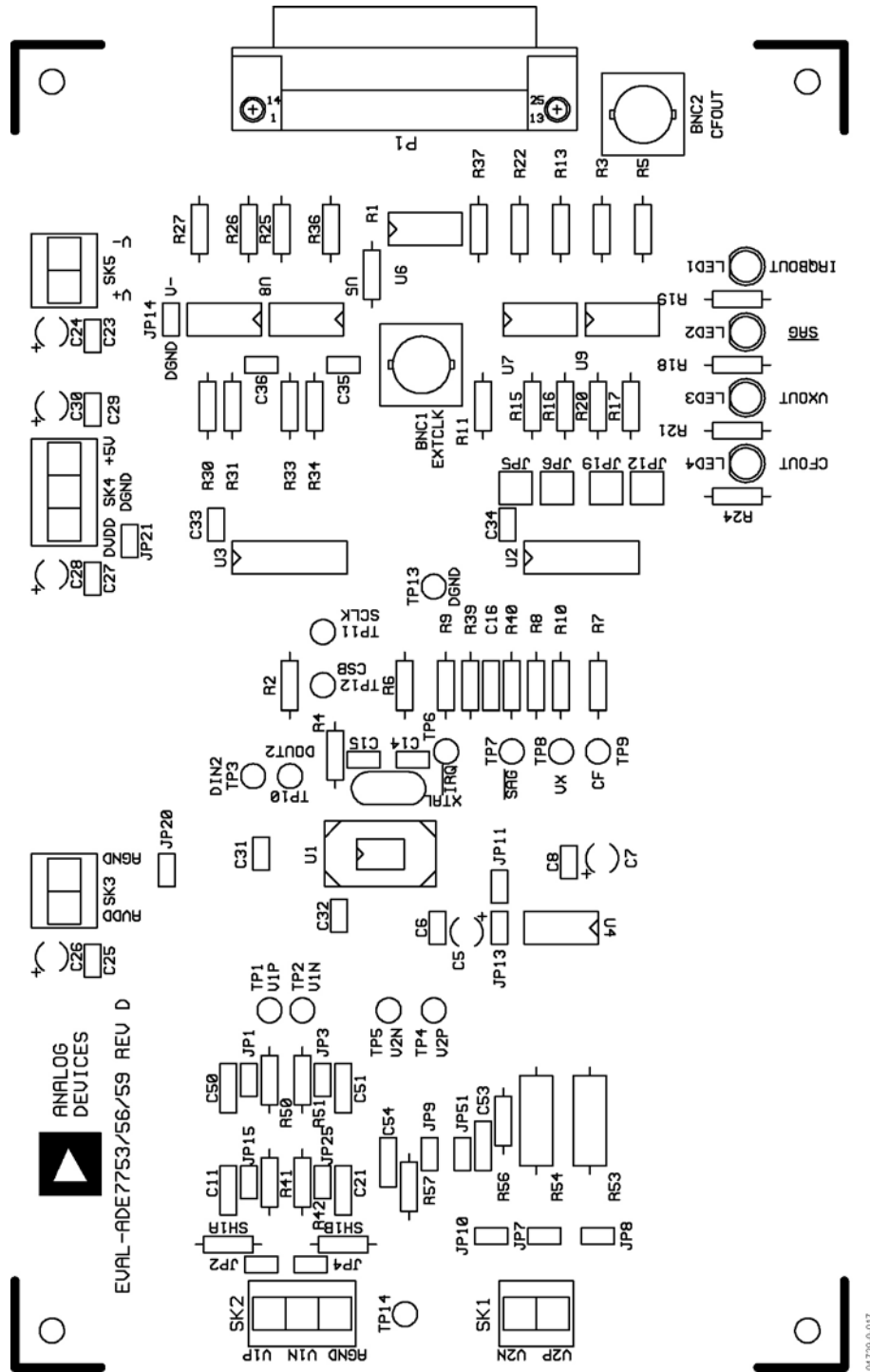
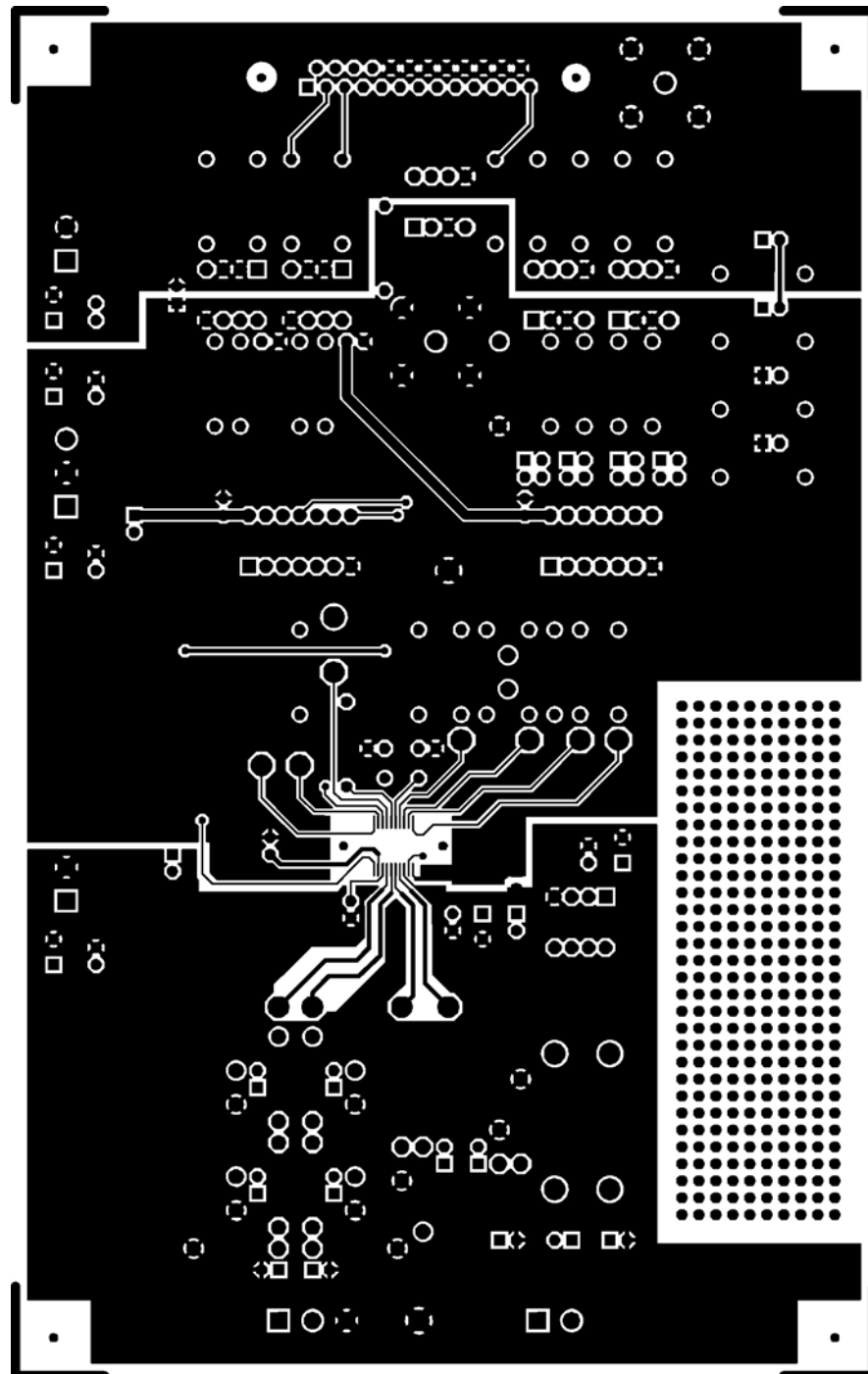


Figure 17. PCB Layout—Component Placement

PCB LAYOUT—COMPONENT SIDE (REV. D)



04729-0-018

Figure 18. PCB Layout—Component Side

PCB LAYOUT—SOLDER SIDE (REV. D)

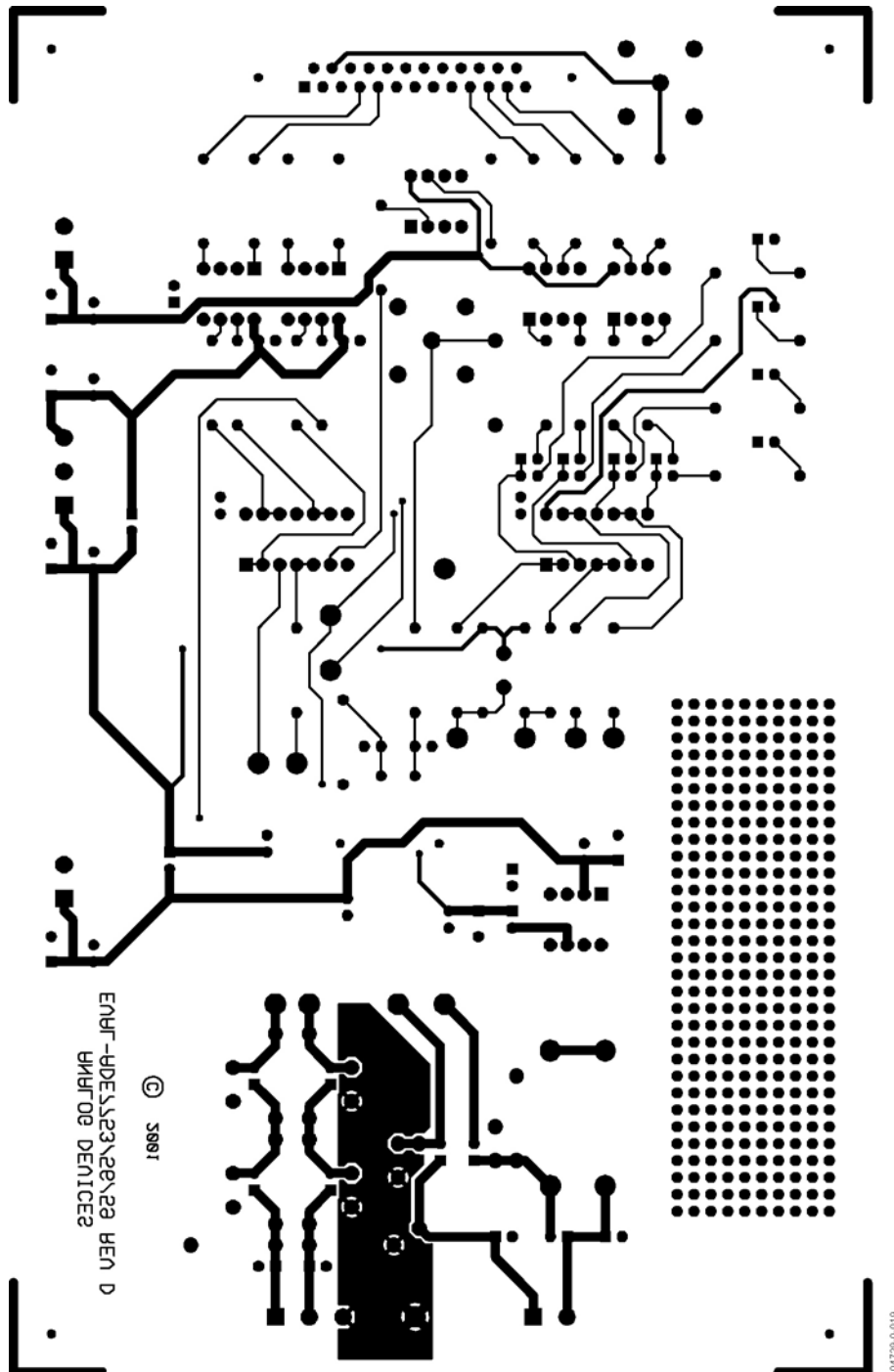


Figure 19. PCB Layout—Solder Side

PCB LAYOUT—COMPONENT PLACEMENT (REV. E)

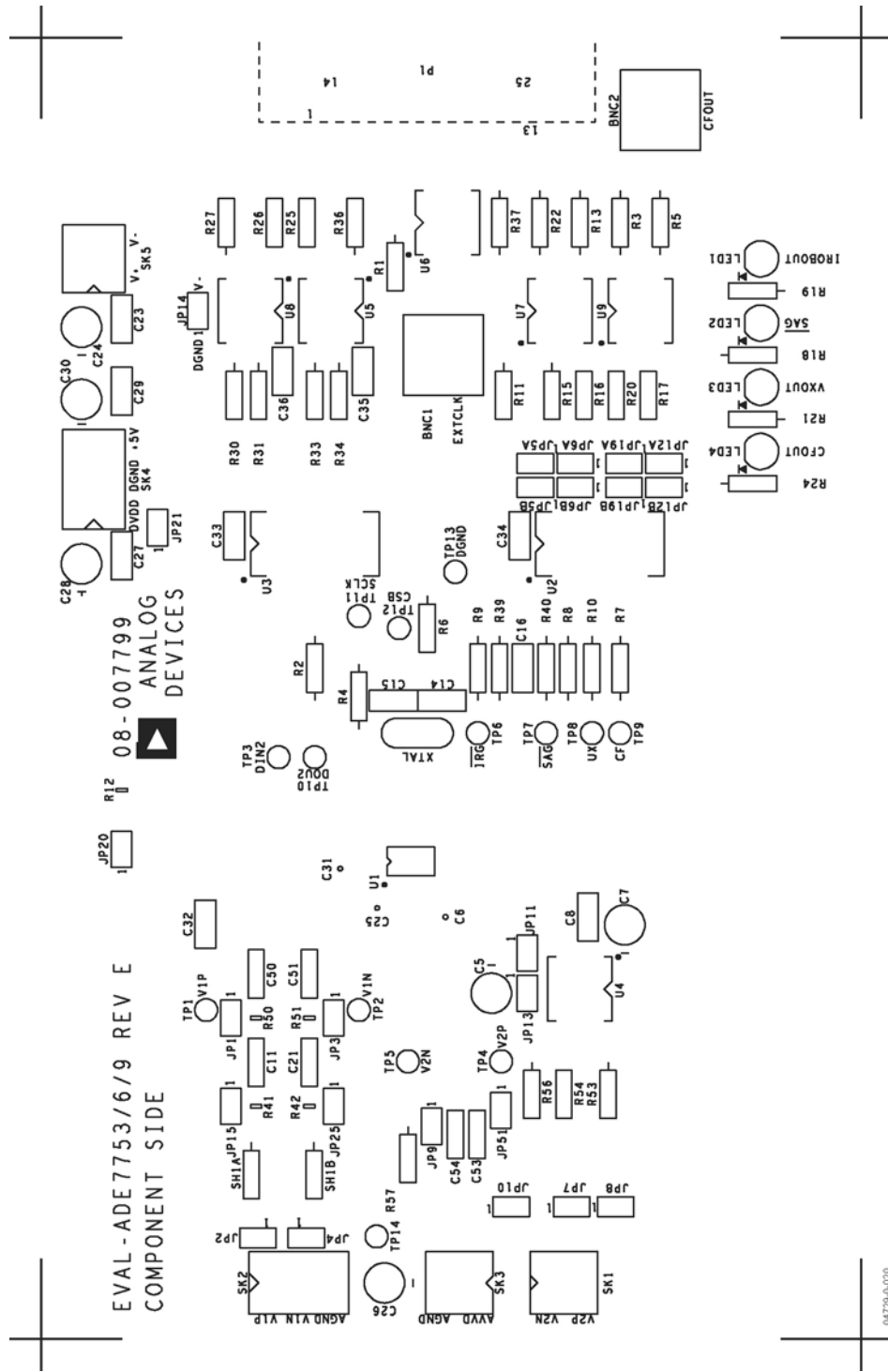


Figure 20. PCB Layout—Component Placement

PCB LAYOUT—COMPONENT SIDE (REV. E)

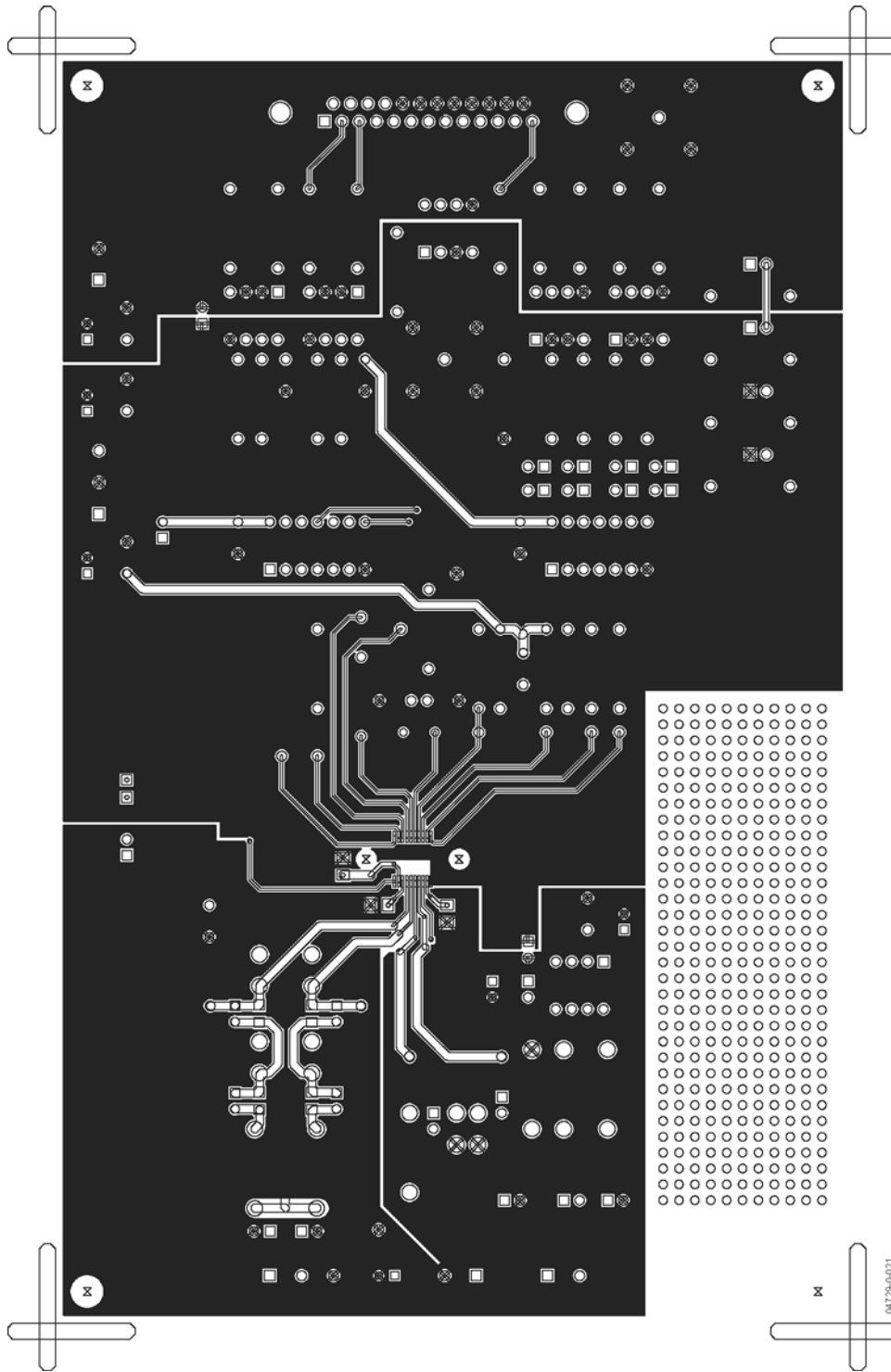


Figure 21. PCB Layout—Component Side

PCB LAYOUT—SOLDER SIDE (REV. E)

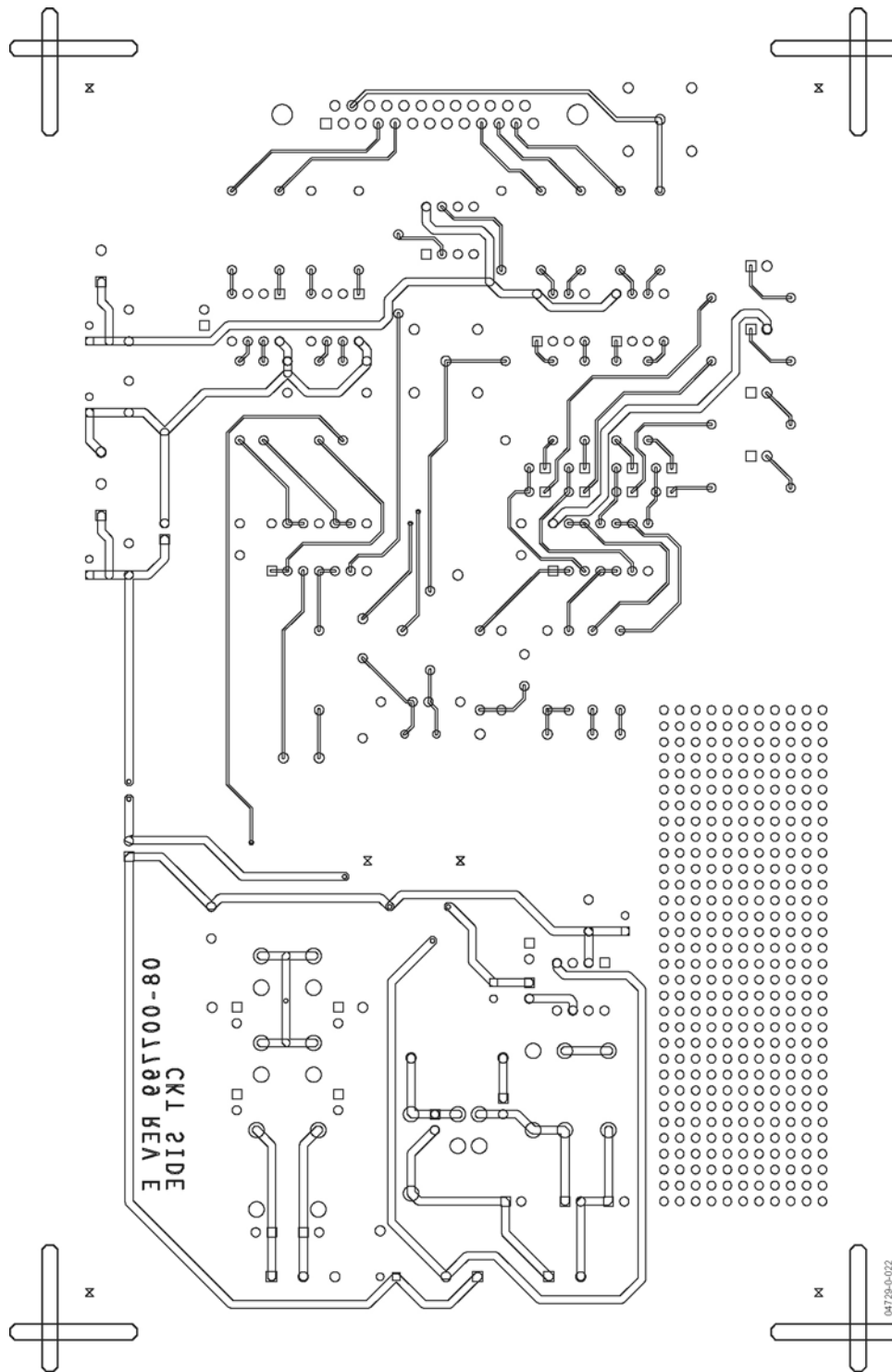


Figure 22. PCB Layout—Solder Side

EVAL-ADE7763EB

ORDERING GUIDE

Model	Description
EVAL-ADE7763EB	Evaluation Board