Fact Sheet

MPC750 AND MPC740 MICROPROCESSORS

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The MPC750 and MPC740 microprocessors are low-power, 32-bit implementations of the PowerPC Reduced Instruction Set Computer (RISC) architecture. The MPC750 and the MPC740 microprocessors differ only in that the MPC750 features a dedicated L2 cache interface with on-chip L2 tags. Both are software-compatible and bus-compatible with the MPC6xx and MPC74xx microprocessors, and the MPC740 is pin-compatible as well. Both microprocessors are fully JTAG-compliant.

SUPERSCALAR MICROPROCESSOR

The MPC750/MPC740 microprocessors are superscalar, capable of issuing three instructions per clock cycle into six independent execution units:

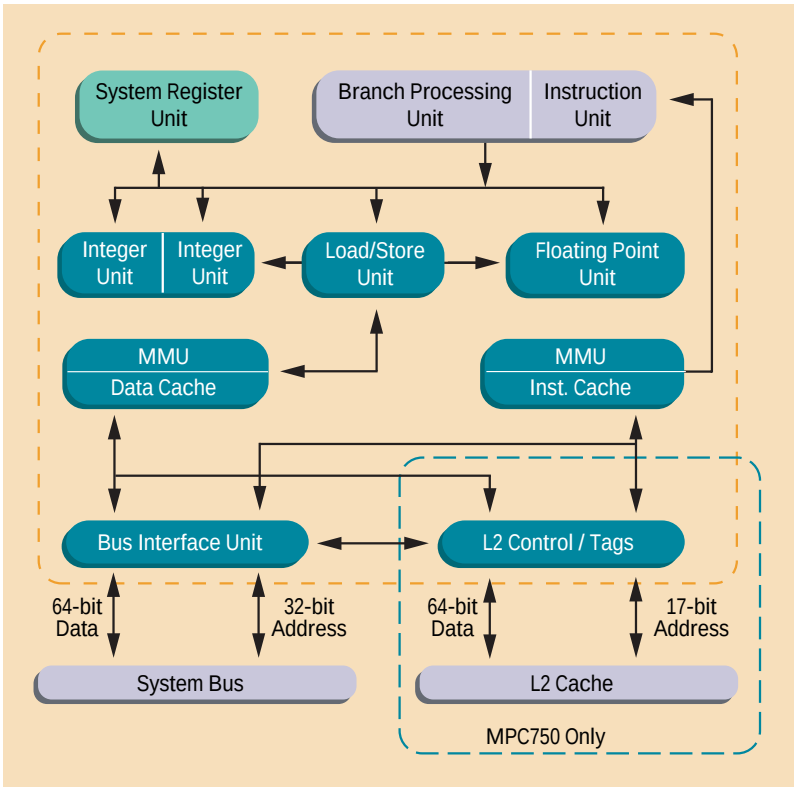
- Two integer units
- Load/store unit
- Floating-point unit
- System register unit
- Branch processing unit

The ability to execute multiple instructions in parallel, the ability to pipeline instructions, and the use of simple instructions with rapid execution times yields maximum efficiency and throughput.

POWER MANAGEMENT

The MPC750/MPC740 microprocessors feature a low-power 2.6V or 1.9V design with three power-saving modes—doze, nap, and sleep. These user-programmable modes progressively reduce the power drawn by the processor. These low-power microprocessors offer dynamic power management to selectively activate functional units as they are needed by the executing instructions. Both microprocessors also provide a thermal assist unit and instruction cache throttling for software-controllable thermal management.

MOTOROLA MPC750/MPC740 BLOCK DIAGRAM



CACHE AND MMU SUPPORT

The MPC750/MPC740 microprocessors have separate 32 KB, physically addressed instruction and data caches. Both caches are eight-way set-associative. The additional dedicated L2 cache interface with on-chip L2 tags (shown below) is provided only by the MPC750 microprocessor. MPC750/MPC740 microprocessors contain separate memory management units (MMUs) for instructions and data, supporting 4 petabytes (2^{52}) of virtual memory and 4 GB (2^{32}) of physical memory. Access privileges and memory protection are controlled on block or page granularities. Large, 128-entry translation lookaside buffers (TLBs) provide efficient physical address translation and support for demand virtual-memory management on both page- and variable-sized blocks.

FLEXIBLE BUS INTERFACE

MPC750/MPC740 microprocessors have a 64-bit data bus and a 32-bit address bus. Support is included for burst, split, and pipelined transactions. The interface provides snooping for data cache coherency. Both microprocessors maintain MEI coherency protocol in hardware, allowing access to system memory for additional caching bus masters, such as DMA devices.

CONTACT INFORMATION

Motorola offers user's manuals, application notes, and sample code for all of its processors. Local support for these products is also provided. This information can be found at: http://motorola.com/smartnetworks

For all other inquiries about Motorola products, please contact the Motorola Customer Response Center at:
Phone: 800-521-6274 or
http://motorola.com/semiconductors

	MPC740 200-266 MHz	MPC740 300-333 MHz	MPC750 200-266 MHz	MPC750 300-400 MHz
CPU Speeds – Internal	200, 233 and 266 MHz	300 and 333 MHz	200, 233 and 266 MHz	300, 333, 366 and 400 MHz
CPU Bus Dividers	x3, x3.5, x4, x4.5, x5, x5.5, x6, x6.5, x7, x7.5, x8	x3, x3.5, x4, x4.5, x5, x5.5, x6, x6.5, x7, x7.5, x8	x3, x3.5, x4, x4.5, x5, x5.5, x6, x6.5, x7, x7.5, x8	x3, x3.5, x4, x4.5, x5, x5.5, x6, x6.5, x7, x7.5, x8
Bus Interface	64-bit	64-bit	64-bit	64-bit
Instructions per Clock	3 (2 + Branch)	3 (2 + Branch)	3 (2 + Branch)	3 (2 + Branch)
L1 Cache	32 KB instruction 32 KB data	32 KB instruction 32 KB data	32 KB instruction 32 KB data	32 KB instruction 32 KB data
L2 Cache	—	—	256, 512 KB 1 MB	256, 512 KB 1 MB
Core-to-L2 Frequency	—	—	1:1, 1.5:1, 2:1, 2.5:1, 3:1	1:1, 1.5:1, 2:1, 2.5:1, 3:1
Typical/Maximum Power Dissipation	5.7W/7.9W @ 266 MHz	4.2W/6.0W @ 333 MHz	5.7W/7.9W @ 266 MHz	5.8W/8.0W @ 400 MHz
Die Size	67 mm^2	67 mm^2	67 mm^2	67 mm^2
Package	255 CBGA	255 CBGA	255 CBGA	255 CBGA
Process	0.29µ 5LM CMOS	0.25µ 5LM CMOS	0.29µ 5LM CMOS	0.25µ 5LM CMOS
Voltage	3.3V I/O, 2.6V internal	3.3V I/O, 1.9V internal	3.3V I/O, 2.6V internal	3.3V I/O, 1.9V internal
SPECint95 (estimated)	11.5 @ 266 MHz	14.4 @ 333 MHz	12.0 @ 266 MHz	18.8 @ 400 MHz
SPECfp95 (estimated)	6.9 @ 266 MHz	8.7 @ 333 MHz	7.4 @ 266 MHz	12.2 @ 400 MHz
Other Performance	488 MIPS @ 266 MHz	610 MIPS @ 333 MHz	488 MIPS @ 266 MHz	733 MIPS @ 400 MHz
Execution Units	Integer, Floating-Point, Branch, Load/Store, System Register	Integer, Floating-Point, Branch, Load/Store, System Register	Integer, Floating-Point, Branch, Load/Store, System Register	Integer, Floating-Point, Branch, Load/Store, System Register

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