National Semiconductor

July 1993

DP83955A/DP83956A LERIC™ LitE Repeater Interface Controller

General Description

The DP83955/56 LitE Repeater Interface Controller (LERIC) may be used to implement an IEEE 802.3 multiport repeater unit. It fully satisfies the IEEE 802.3 repeater specification including the functions defined by the repeater, segment partition and jabber lockup protection state machines.

The LERIC has an on-chip phase-locked-loop (PLL) for Manchester data decoding, a Manchester encoder, and an Elasticity Buffer for preamble regeneration.

Each LERIC can connect up to 7 cable segments via its network interface ports. One port is fully Attachment Unit Interface (AUI) compatible and is able to connect to an external Medium Attachment Unit (MAU) using the maximum length of AUI cable. The other 6 ports have integrated 10BASE-T transceivers. These transceiver functions may be bypassed so that the LERIC may be used with external transceivers, such as National's DP8392 coaxial transceiver. In addition, large repeater units may be constructed by cascading LERICs together over the Inter-LERIC™ or Inter-RIC™ bus.

The LERIC is configurable for specific applications. It provides port status information for LED array displays. Additionally, the LERIC has a μP interface to provide individual port status, configuration, and port enable/disable functions.

The DP83956 has all the features of the DP83955, except that two of the bidirectional signals on DP83955 are changed to unidirectional signals on DP83956, and one more signal is added to DP83956 to accommodate the addition of bus transceivers for cascading a greater number of LERICs in large repeater applications.

Specifications enclosed describe both the DP83955 and the DP83956 unless otherwise noted.

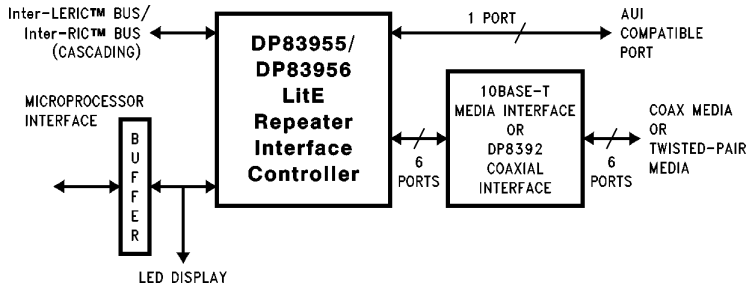
For IEEE 802.3 multiport repeater applications which require conformance to the IEEE 802.3 Draft Repeater Management options, the DP83950 Repeater Interface Controller (RIC™) is recommended especially for highly-managed hub requirements.

Features

- Compliant with the IEEE 802.3 Repeater Specification
- 7 network connections (ports) per chip
- Selectable on-chip twisted-pair transceivers
- Cascadable for large multiple RIC/LERIC hub applications
- Compatible with AUI compliant transceivers
- On-chip Elasticity Buffer, Manchester encoder and decoder
- Separation Partition state machines for each port
- Provides port status information for LED displays including: receive, collision, partition, polarity, and link status
- Power-up configuration options—Repeater and Partition Specifications, Transceiver Interface, Status Display, Processor Operations
- Simple processor interface for repeater management and port disable
- Per port receive squelch level selection
- CMOS process for low power dissipation
- Single 5V supply

1.0 System Diagram

Simple LERIC Hub



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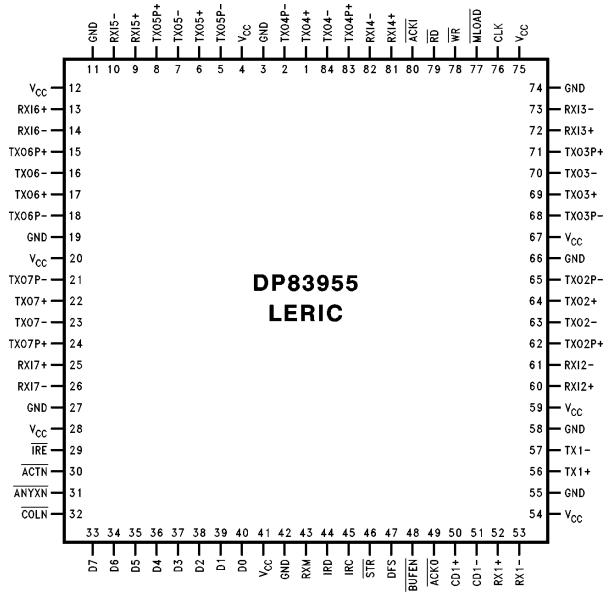
2.0 Connection Diagrams

Pin Table for DP83955
(Configured as Port 1 Full AUI, and Ports 2–7 Twisted-Pair)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
TXO4+	1	TXO7+	22	RXM	43	TXO2+	64
TXO4P−	2	TXO7−	23	IRD	44	TXO2P−	65
GND	3	TXO7P+	24	IRC	45	GND	66
V_{CC}	4	RXI7+	25	$\overline{STR}$	46	V_{CC}	67
TXO5P−	5	RXI7−	26	DFS	47	TXO3P−	68
TXO5+	6	GND	27	$\overline{BUFEN}$	48	TXO3+	69
TXO5−	7	V_{CC}	28	$\overline{ACKO}$	49	TXO3−	70
TXO5P+	8	$\overline{IRE}$	29	CD1+	50	TXO3P+	71
RXI5+	9	$\overline{ACTN}$	30	CD1−	51	RXI3+	72
RXI5−	10	$\overline{ANYXN}$	31	RX1+	52	RXI3−	73
GND	11	$\overline{COLN}$	32	RX1−	53	GND	74
V_{CC}	12	D7	33	V_{CC}	54	V_{CC}	75
RXI6+	13	D6	34	GND	55	CLK	76
RXI6−	14	D5	35	TX1+	56	$\overline{MLOAD}$	77
TXO6P+	15	D4	36	TX1−	57	$\overline{WR}$	78
TXO6−	16	D3	37	GND	58	$\overline{RD}$	79
TXO6+	17	D2	38	V_{CC}	59	$\overline{ACKI}$	80
TXO6P−	18	D1	39	RXI2+	60	RXI4+	81
GND	19	D0	40	RXI2−	61	RXI4−	82
V_{CC}	20	V_{CC}	41	TXO2P+	62	TXO4P+	83
TXO7P−	21	GND	42	TXO2−	63	TXO4−	84



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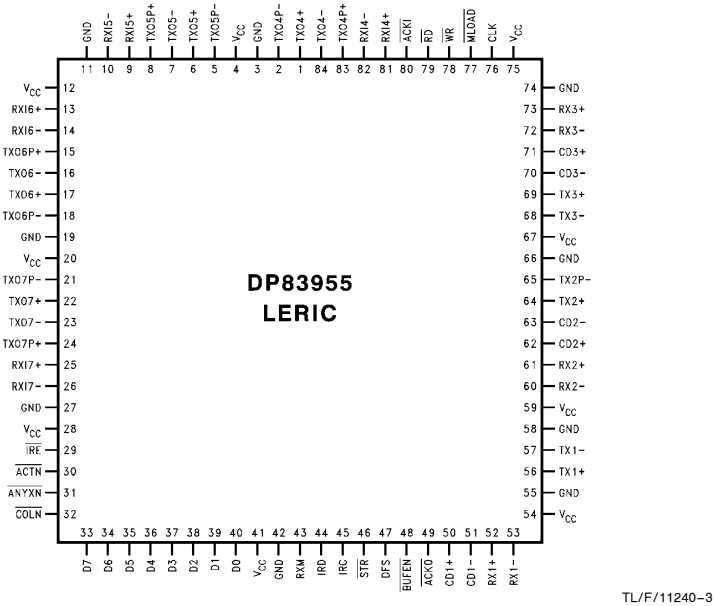
Top View

2.0 Connection Diagrams (Continued)

Pin Table for DP83955
(Configured as Port 1 Full AUI, Ports 2–3 AUI, and Ports 4–7 Twisted-Pair)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
TXO4+	1	TXO7+	22	RXM	43	TX2+	64
TXO4P−	2	TXO7−	23	IRD	44	TX2−	65
GND	3	TXO7P+	24	IRC	45	GND	66
V_{CC}	4	RXI7+	25	$\overline{STR}$	46	V_{CC}	67
TXO5P−	5	RXI7−	26	DFS	47	TX3−	68
TXO5+	6	GND	27	$\overline{BUFEN}$	48	TX3+	69
TXO5−	7	V_{CC}	28	$\overline{ACKO}$	49	CD3−	70
TXO5P+	8	$\overline{IRE}$	29	CD1+	50	CD3+	71
RXI5+	9	$\overline{ACTN}$	30	CD1−	51	RX3−	72
RXI5−	10	$\overline{ANYXN}$	31	RX1+	52	RX3+	73
GND	11	$\overline{COLN}$	32	RX1−	53	GND	74
V_{CC}	12	D7	33	V_{CC}	54	V_{CC}	75
RXI6+	13	D6	34	GND	55	CLK	76
RXI6−	14	D5	35	TX1+	56	$\overline{MLOAD}$	77
TXO6P+	15	D4	36	TX1−	57	$\overline{WR}$	78
TXO6−	16	D3	37	GND	58	$\overline{RD}$	79
TXO6+	17	D2	38	V_{CC}	59	$\overline{ACKI}$	80
TXO6P−	18	D1	39	RX2−	60	RXI4+	81
GND	19	D0	40	RX2+	61	RXI4−	82
V_{CC}	20	V_{CC}	41	CD2+	62	TXO4P+	83
TXO7P−	21	GND	42	CD2−	63	TXO4−	84



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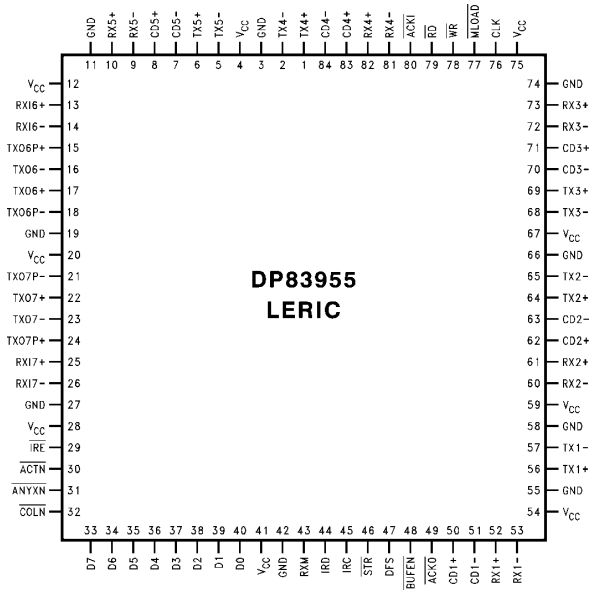
Top View

2.0 Connection Diagrams (Continued)

Pin Table for DP83955
(Configured as Port 1 Full AUI, Ports 2–5 AUI, and Ports 6–7 Twisted-Pair)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
TX4+	1	TXO7+	22	RXM	43	TX2+	64
TX4−	2	TXO7−	23	IRD	44	TX2−	65
GND	3	TXO7P+	24	IRC	45	GND	66
V_{CC}	4	RXI7+	25	$\overline{STR}$	46	V_{CC}	67
TX5−	5	RXI7−	26	DFS	47	TX3−	68
TX5+	6	GND	27	$\overline{BUFEN}$	48	TX3+	69
CD5−	7	V_{CC}	28	$\overline{ACKO}$	49	CD3−	70
CD5+	8	$\overline{IRE}$	29	CD1+	50	CD3+	71
RX5−	9	$\overline{ACTN}$	30	CD1−	51	RX3−	72
RX5+	10	$\overline{ANYXN}$	31	RX1+	52	RX3+	73
GND	11	$\overline{COLN}$	32	RX1−	53	GND	74
V_{CC}	12	D7	33	V_{CC}	54	V_{CC}	75
RXI6+	13	D6	34	GND	55	CLK	76
RXI6−	14	D5	35	TX1+	56	$\overline{MLOAD}$	77
TXO6P+	15	D4	36	TX1−	57	$\overline{WR}$	78
TXO6−	16	D3	37	GND	58	$\overline{RD}$	79
TXO6+	17	D2	38	V_{CC}	59	$\overline{ACKI}$	80
TXO6P−	18	D1	39	RX2−	60	RX4−	81
GND	19	D0	40	RX2+	61	RX4+	82
V_{CC}	20	V_{CC}	41	CD2+	62	CD4+	83
TXO7P−	21	GND	42	CD2−	63	CD4−	84



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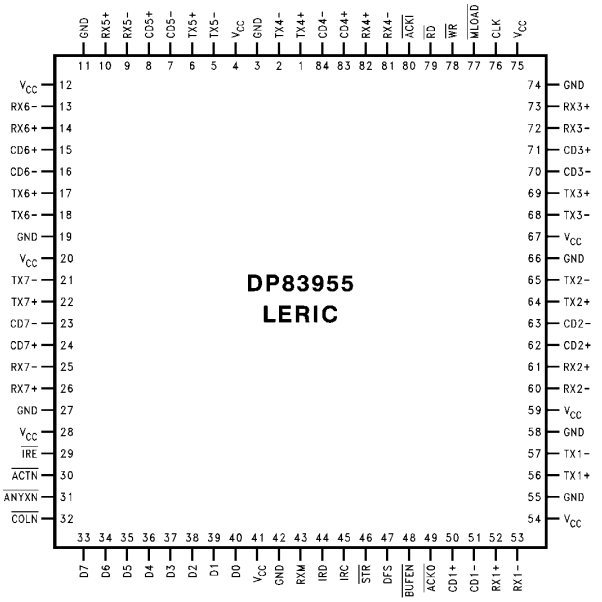
Top View

2.0 Connection Diagrams (Continued)

Pin Table for DP83955
(Configured as Port 1 Full AUI, Ports 2–7 AUI)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
TX4+	1	TX7+	22	RXM	43	TX2+	64
TX4−	2	CD7−	23	IRD	44	TX2−	65
GND	3	CD7+	24	IRC	45	GND	66
V_{CC}	4	RX7−	25	$\overline{STR}$	46	V_{CC}	67
TX5−	5	RX7+	26	DFS	47	TX3−	68
TX5+	6	GND	27	$\overline{BUFEN}$	48	TX3+	69
CD5−	7	V_{CC}	28	$\overline{ACKO}$	49	CD3−	70
CD5+	8	$\overline{IRE}$	29	CD1+	50	CD3+	71
RX5−	9	$\overline{ACTN}$	30	CD1−	51	RX3−	72
RX5+	10	$\overline{ANYXN}$	31	RX1+	52	RX3+	73
GND	11	$\overline{COLN}$	32	RX1−	53	GND	74
V_{CC}	12	D7	33	V_{CC}	54	V_{CC}	75
RX6−	13	D6	34	GND	55	CLK	76
RX6+	14	D5	35	TX1+	56	$\overline{MLOAD}$	77
CD6+	15	D4	36	TX1−	57	$\overline{WR}$	78
CD6−	16	D3	37	GND	58	$\overline{RD}$	79
TX6+	17	D2	38	V_{CC}	59	$\overline{ACKI}$	80
TX6−	18	D1	39	RX2−	60	RX4−	81
GND	19	D0	40	RX2+	61	RX4+	82
V_{CC}	20	V_{CC}	41	CD2+	62	CD4+	83
TX7−	21	GND	42	CD2−	63	CD4−	84



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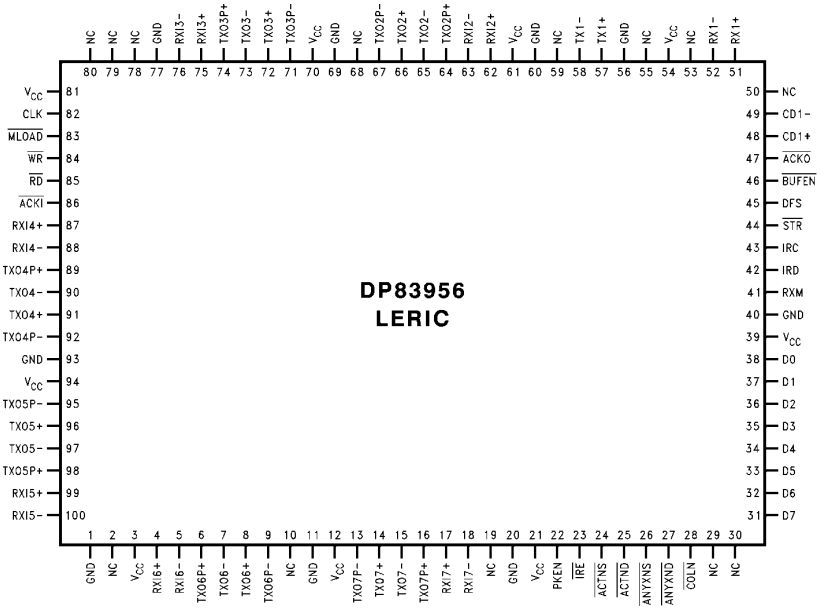
Top View

2.0 Connection Diagrams (Continued)

Pin Table for DP83956
(Configured as Port 1 Full AUI, Ports 2–7 Twisted-Pair)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
GND	1	V_{CC}	21	RXM	41	V_{CC}	61	V_{CC}	81
NC	2	PKEN	22	IRD	42	RXI2+	62	CLK	82
V_{CC}	3	$\overline{IRE}$	23	IRC	43	RXI2−	63	$\overline{MLOAD}$	83
RXI6+	4	$\overline{ACTNS}$	24	$\overline{STR}$	44	TXO2P+	64	$\overline{WR}$	84
RXI6−	5	$\overline{ACTND}$	25	DFS	45	TXO2−	65	$\overline{RD}$	85
TXO6P+	6	$\overline{ANYXNS}$	26	$\overline{BUFEN}$	46	TXO2+	66	$\overline{ACKI}$	86
TXO6−	7	$\overline{ANYXND}$	27	$\overline{ACKO}$	47	TXO2P−	67	RXI4+	87
TXO6+	8	$\overline{COLN}$	28	CD1+	48	NC	68	RXI4−	88
TXO6P−	9	NC	29	CD1−	49	GND	69	TXO4P+	89
NC	10	NC	30	NC	50	V_{CC}	70	TXO4−	90
GND	11	D7	31	RX1+	51	TXO3P−	71	TXO4+	91
V_{CC}	12	D6	32	RX1−	52	TXO3+	72	TXO4P−	92
TXO7P−	13	D5	33	NC	53	TXO3−	73	GND	93
TXO7+	14	D4	34	V_{CC}	54	TXO3P+	74	V_{CC}	94
TXO7−	15	D3	35	NC	55	RXI3+	75	TXO5P−	95
TXO7P+	16	D2	36	GND	56	RXI3−	76	TXO5+	96
RXI7+	17	D1	37	TX1+	57	GND	77	TXO5−	97
RXI7−	18	D0	38	TX1−	58	NC	78	TXO5P+	98
NC	19	V_{CC}	39	NC	59	NC	79	RXI5+	99
GND	20	GND	40	GND	60	NC	80	RXI5−	100

Note: DP83956 will change from VLY package to VLJ package approximately Q3, 1993.



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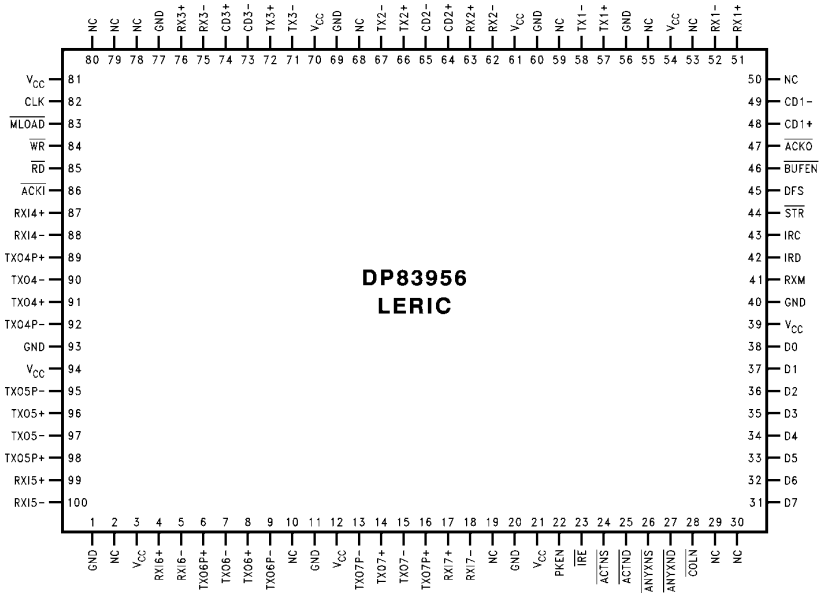
Top View

2.0 Connection Diagrams (Continued)

Pin Table for DP83956
(Configured as Port 1 Full AUI, Ports 2–3, AUI and Ports 4–7 Twisted-Pair)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
GND	1	V_{CC}	21	RXM	41	V_{CC}	61	V_{CC}	81
NC	2	PKEN	22	IRD	42	RX2−	62	CLK	82
V_{CC}	3	$\overline{IRE}$	23	IRC	43	RX2+	63	$\overline{MLOAD}$	83
RXI6+	4	$\overline{ACTNS}$	24	$\overline{STR}$	44	CD2+	64	$\overline{WR}$	84
RXI6−	5	$\overline{ACTND}$	25	DFS	45	CD2−	65	$\overline{RD}$	85
TXO6P+	6	$\overline{ANYXNS}$	26	$\overline{BUFEN}$	46	TX2+	66	$\overline{ACKI}$	86
TXO6−	7	$\overline{ANYXND}$	27	$\overline{ACKO}$	47	TX2−	67	RXI4+	87
TXO6+	8	$\overline{COLN}$	28	CD1+	48	NC	68	RXI4−	88
TXO6P−	9	NC	29	CD1−	49	GND	69	TXO4P+	89
NC	10	NC	30	NC	50	V_{CC}	70	TXO4−	90
GND	11	D7	31	RX1+	51	TX3−	71	TXO4+	91
V_{CC}	12	D6	32	RX1−	52	TX3+	72	TXO4P−	92
TXO7P−	13	D5	33	NC	53	CD3−	73	GND	93
TXO7+	14	D4	34	V_{CC}	54	CD3+	74	V_{CC}	94
TXO7−	15	D3	35	NC	55	RX3−	75	TXO5P−	95
TXO7P+	16	D2	36	GND	56	RX3+	76	TXO5+	96
RXI7+	17	D1	37	TX1+	57	GND	77	TXO5−	97
RXI7−	18	D0	38	TX1−	58	NC	78	TXO5P+	98
NC	19	V_{CC}	39	NC	59	NC	79	RXI5+	99
GND	20	GND	40	GND	60	NC	80	RXI5−	100

Note: DP83956 will change from VLY package to VLJ package approximately Q3, 1993.



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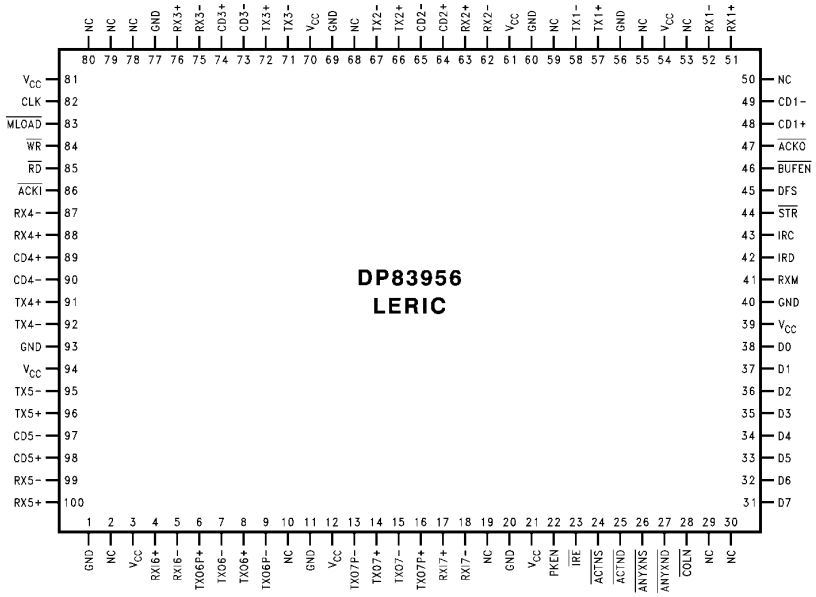
Top View

2.0 Connection Diagrams (Continued)

Pin Table for DP83956
(Configured as Port 1 Full AUI, Ports 2–5, AUI, and Ports 6–7 Twisted-Pair)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
GND	1	V_{CC}	21	RXM	41	V_{CC}	61	V_{CC}	81
NC	2	PKEN	22	IRD	42	RX2−	62	CLK	82
V_{CC}	3	$\overline{IRE}$	23	IRC	43	RX2+	63	$\overline{MLOAD}$	83
RXI6+	4	$\overline{ACTNS}$	24	$\overline{STR}$	44	CD2+	64	$\overline{WR}$	84
RXI6−	5	$\overline{ACTND}$	25	DFS	45	CD2−	65	$\overline{RD}$	85
TXO6P+	6	$\overline{ANYXNS}$	26	$\overline{BUFEN}$	46	TX2+	66	$\overline{ACKI}$	86
TXO6−	7	$\overline{ANYXND}$	27	$\overline{ACKO}$	47	TX2−	67	RX4−	87
TXO6+	8	$\overline{COLN}$	28	CD1+	48	NC	68	RX4+	88
TXO6P−	9	NC	29	CD1−	49	GND	69	CD4+	89
NC	10	NC	30	NC	50	V_{CC}	70	CD4−	90
GND	11	D7	31	RX1+	51	TX3−	71	TX4+	91
V_{CC}	12	D6	32	RX1−	52	TX3+	72	TX4−	92
TXO7P−	13	D5	33	NC	53	CD3−	73	GND	93
TXO7+	14	D4	34	V_{CC}	54	CD3+	74	V_{CC}	94
TXO7−	15	D3	35	NC	55	RX3+	75	TX5−	95
TXO7P+	16	D2	36	GND	56	RX3−	76	TX5+	96
RXI7+	17	D1	37	TX1+	57	GND	77	CD5−	97
RXI7−	18	D0	38	TX1−	58	NC	78	CD5+	98
NC	19	V_{CC}	39	NC	59	NC	79	RX5−	99
GND	20	GND	40	GND	60	NC	80	RX5+	100

Note: DP83956 will change from VLY package to VLJ package approximately Q3, 1993.



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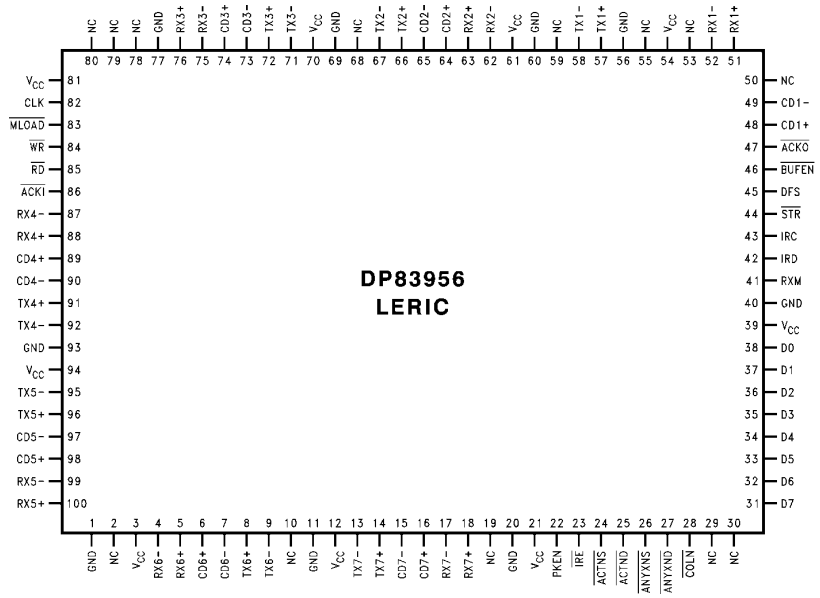
Top View

2.0 Connection Diagrams (Continued)

Pin Table for DP83956
(Configured as Port 1 Full AUI, Ports 2–7 AUI)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
GND	1	V_{CC}	21	RXM	41	V_{CC}	61	V_{CC}	81
NC	2	PKEN	22	IRD	42	RX2−	62	CLK	82
V_{CC}	3	$\overline{IRE}$	23	IRC	43	RX2+	63	$\overline{MLOAD}$	83
RX6−	4	$\overline{ACTNS}$	24	$\overline{STR}$	44	CD2+	64	$\overline{WR}$	84
RX6+	5	$\overline{ACTND}$	25	DFS	45	CD2−	65	$\overline{RD}$	85
CD6+	6	$\overline{ANYXNS}$	26	$\overline{BUFEN}$	46	TX2+	66	$\overline{ACKI}$	86
CD6−	7	$\overline{ANYXND}$	27	$\overline{ACKO}$	47	TX2−	67	RX4−	87
TX6+	8	$\overline{COLN}$	28	CD1+	48	NC	68	RX4+	88
TX6−	9	NC	29	CD1−	49	GND	69	CD4+	89
NC	10	NC	30	NC	50	V_{CC}	70	CD4−	90
GND	11	D7	31	RX1+	51	TX3−	71	TX4+	91
V_{CC}	12	D6	32	RX1−	52	TX3+	72	TX4−	92
TX7−	13	D5	33	NC	53	CD3−	73	GND	93
TX7+	14	D4	34	V_{CC}	54	CD3+	74	V_{CC}	94
CD7−	15	D3	35	NC	55	RX3+	75	TX5−	95
CD7+	16	D2	36	GND	56	RX3−	76	TX5+	96
RX7−	17	D1	37	TX1+	57	GND	77	CD5−	97
RX7+	18	D0	38	TX1−	58	NC	78	CD5+	98
NC	19	V_{CC}	39	NC	59	NC	79	RX5+	99
GND	20	GND	40	GND	60	NC	80	RX5−	100

Note: DP83956 will change from VLY package to VLJ package approximately Q3, 1993.



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Top View

3.0 Pin Description

Pin Name	Driver Type	I/O	Description
NETWORK INTERFACE PINS (**On-Chip** Transceiver Mode)			
RXI2− to RXI7−	TP	I	Twisted-Pair **R**eceive **I**nput Negative
RXI2+ to RXI7+	TP	I	Twisted-Pair **R**eceive **I**nput Positive
TXOP2− to TXOP7−	TT	O	Twisted-Pair **P**re-Emphasis **T**ransmit **O**utput Negative
TXO2− to TXO7−	TT	O	Twisted-Pair **T**ransmit **O**utput Negative
TXO2+ to TXO7+	TT	O	Twisted-Pair **T**ransmit **O**utput Positive
TXOP2+ to TXOP7+	TT	O	Twisted-Pair **P**re-Emphasis **T**ransmit **O**utput Positive
CD1+	AL	I	AUI **C**ollision **D**etect Input Positive
CD1−	AL	I	AUI **C**ollision **D**etect Input Negative
RX1+	AL	I	AUI **R**eceive Input Positive
RX1−	AL	I	AUI **R**eceive Input Negative
TX1+	AD	O	AUI **T**ransmit Output Positive
TX1−	AD	O	AUI **T**ransmit Output Negative
NETWORK INTERFACE PINS (**External** Transceiver Mode **AUI Signal Level Compatibility Selected**)			
TX2+ to TX7+	AL	O	**T**ransmit Output Positive
TX2− to TX7−	AL	O	**T**ransmit Output Negative
CD2+ to CD7+	AL	I	**C**ollision Input Positive
CD2− to CD7−	AL	I	**C**ollision Input Negative
RX2+ to RX7+	AL	I	**R**eceive Input Positive
RX2− to RX7−	AL	I	**R**eceive Input Negative
CD1+	AL	I	AUI **C**ollision **D**etect Input Positive
CD1−	AL	I	AUI **C**ollision **D**etect Input Negative
RX1+	AL	I	AUI **R**eceive Input Positive
RX1−	AL	I	AUI **R**eceive Input Negative
TX1+	AD	O	AUI **T**ransmit Output Positive
TX1−	AD	O	AUI **T**ransmit Output Negative

Note: **AD** = **A**UI level and **D**rive compatible
TP = **T**wisted-**P**air interface compatible
AL = **A**UI **L**evel compatible
TT = **TT**L compatible
I = **I**nput
O = **O**utput

3.0 Pin Description (Continued)

Pin Name	Driver Type	I/O	Description
PROCESSOR BUS PINS			
$\overline{STR}$	C	O	Display Update **STR**obe: This signal controls the latching of display data for network ports into the off chip display latches. During processor access cycles (read or write is asserted) this signal is inactive (high).
D(7:0)	TT	B, Z	**D**ata Bus: **Display Update Cycles:** These pins become outputs providing display data and port address information. **Processor Access Cycles:** Address input **D**(7:4) and Data input or output **D**(3:0) is performed via these pins. The read, write and reset inputs control the direction of the signals. **Note:** The data pins remain in their display update function, (i.e., asserted as outputs) unless either the read or write strobe is asserted.
DFS	C	O	**D**isplay **F**rozen **S**trobe: The assertion of the DFS signal, active high, at the end of the transmission of each packet indicates that the status of that packet is frozen on the LEDs until the beginning of the next received packet or for a maximum of 30 ms.
$\overline{BUFEN}$	C	O	**BUF**fer **EN**able: This output controls the TRI-STATE® operation of the bus transceiver which provides the interface between the LERIC's data pins and the processor's data bus. **Note:** The buffer enable output indicates the function of the data pins. When it is high they are performing display update cycles, when it is low a processor access or $\overline{MLOAD}$ cycle is occurring.
$\overline{WR}$	TT	I	**WR**ite Strobe: Strobe from the CPU used to write an internal register defined by the **D**(7:4) inputs.
$\overline{RD}$	TT	I	**R**ea**D** Strobe: Strobe from the CPU used to read an internal register defined by the **D**(7:4) inputs.
$\overline{MLOAD}$	TT	I	Device **MLOAD** and Reset: When this input is low all of the RIC's state machines and network ports are reset and held inactive. On the rising edge of $\overline{MLOAD}$ the logic levels present on the **D**(7:0) pins are latched into the LERIC's configuration registers. The rising edge of $\overline{MLOAD}$ also signals the beginning of the display test operation.
INTER-LERIC BUS PINS			
$\overline{ACKI}$	TT	I	**ACK**nowledge **I**nput: Input to the network ports' arbitration chain.
$\overline{ACKO}$	TT	O	**ACK**nowledge **O**utput: Output from the network ports' arbitration chain.
IRD	TT	B, Z	**I**nter-LE**R**IC **D**ata: When asserted as an output this signal provides a serial data stream in NRZ format. The signal is asserted by a LERIC when it is receiving data from one of its network segments. The default condition of this signal is to be an input. In this state it may be driven by other devices on the Inter-LERIC bus.

3.0 Pin Description (Continued)

Pin Name	Driver Type	I/O	Description
INTER-LERIC BUS PINS (Continued)			
$\overline{IRE}$	TT	B, Z	**I**nter-LE**R**IC **E**nable: When asserted as an output this signal provides an activity framing enable for the serial data stream. The signal is asserted by a LERIC when it is receiving data from one of its network segments. The default condition of this signal is to be an input. In this state it may be driven by other devices on the Inter-LERIC bus.
IRC	TT	B, Z	**I**nter-LE**R**IC **C**lock: When asserted as an output this signal provides a clock signal for the serial data stream. Data (IRD) is changed on the falling edge of the clock. The signal is asserted by a LERIC when it is receiving data from one of its network segments. The default condition of this signal is to be an input. When an input, IRD is sampled on the rising edge of the clock. In this state it may be driven by other devices on the Inter-LERIC bus.
$\overline{COLN}$	TT	B, Z	**COL**lision on Port **N**: This denotes that a collision is occurring on the port receiving the data packet (Port N). The default condition of this signal is to be an input. In this state it may be driven by other devices on the Inter-LERIC bus.
CLK	TT	I	20 MHz Clock Input: This input is used to generate the LERIC's timing reference for the state machines, and phase lock loop decoder. The 20 MHz clock should have a 0.01% frequency tolerance and 40%–60% duty cycle or better (i.e. 50/50 duty cycle).
POWER AND GROUND PINS			
V_{CC}			Positive Supply
GND			Negative Supply
EXTERNAL DECODER PINS			
RXM	TT	O	**Receive Data Manchester Format:** This output makes the data, in Manchester format, received by port N available for test purposes. If not used for testing, this pin should be left open.

Note: **TT** = **TT**L compatible
B = **B**i-directional
C = **C**MOS compatible
OD = **O**pen **D**rain
I = **I**nput
O = **O**utput
Z = TRI-STATE

3.0 Pin Description (Continued)

Pin Description for DP83955

Pin No.	Pin Name	Driver Type	I/O	Description
30	$\overline{\text{ACTN}}$	OD	B	**ACT**ivity on Port **N**: This is a bidirectional signal. The LERIC asserts this signal when data or collision information is received from one of its network segments. The LERIC senses this signal when this LERIC or another LERIC in a multi-LERIC system is receiving data or collision information.
31	$\overline{\text{ANYXN}}$	OD	B	**A**ctivity on A**NY** Port E**X**cluding Port **N**: This is a bidirectional signal. The LERIC asserts this signal when a transmit collision is experienced or multiple ports have active collisions on their network segments. The LERIC senses this signal when this LERIC or other LERICs in a multi-LERIC system are experiencing transmit collisions or multiple ports have active collisions on their network segments.

B = **B**i-directional

Pin Description for DP83956

Pin No.	Pin Name	Driver Type	I/O	Description
25	$\overline{\text{ACTND}}$	OD	O	**ACT**ivity on Port **N D**rive: The LERIC asserts this signal when data or collision information is received from one of its network segments.
24	$\overline{\text{ACTNS}}$	TT	I	**ACT**ivity on Port **N S**ense: The LERIC senses this signal when this LERIC or another LERIC in a multi-LERIC system is receiving data or collision information.
27	$\overline{\text{ANYXND}}$	OD	O	**A**ctivity on A**NY** Port E**X**cluding Port **N D**rive: The LERIC asserts this signal when a transmit collision is experienced or multiple ports have active collisions on their network segments.
26	$\overline{\text{ANYXNS}}$	TT	I	**A**ctivity on A**NY** Port E**X**cluding Port **N S**ense: The LERIC senses this signal when this LERIC or other LERICs in a multi-LERIC system are experiencing transmit collisions or multiple ports have active collisions on their network segments.
22	PKEN	C	O	**P**ac**K**et **EN**able: This signal acts as an active high enable for an external bus transceiver (if required) for the IRE, IRC, IRD, and COLN signals. When high, the bus transceiver should be transmitting on to the bus, i.e., this LERIC is driving the IRD, IRE, IRC, and COLN bus lines. When low, the bus transceiver should receive from the bus.

TT = **TTL** compatible, **C** = **C**MOS compatible, **OD** = **O**pen **D**rain, **I** = **I**nput, **O** = **O**utput

4.0 Block Diagram

4.0.1 DP83955 BLOCK DIAGRAM

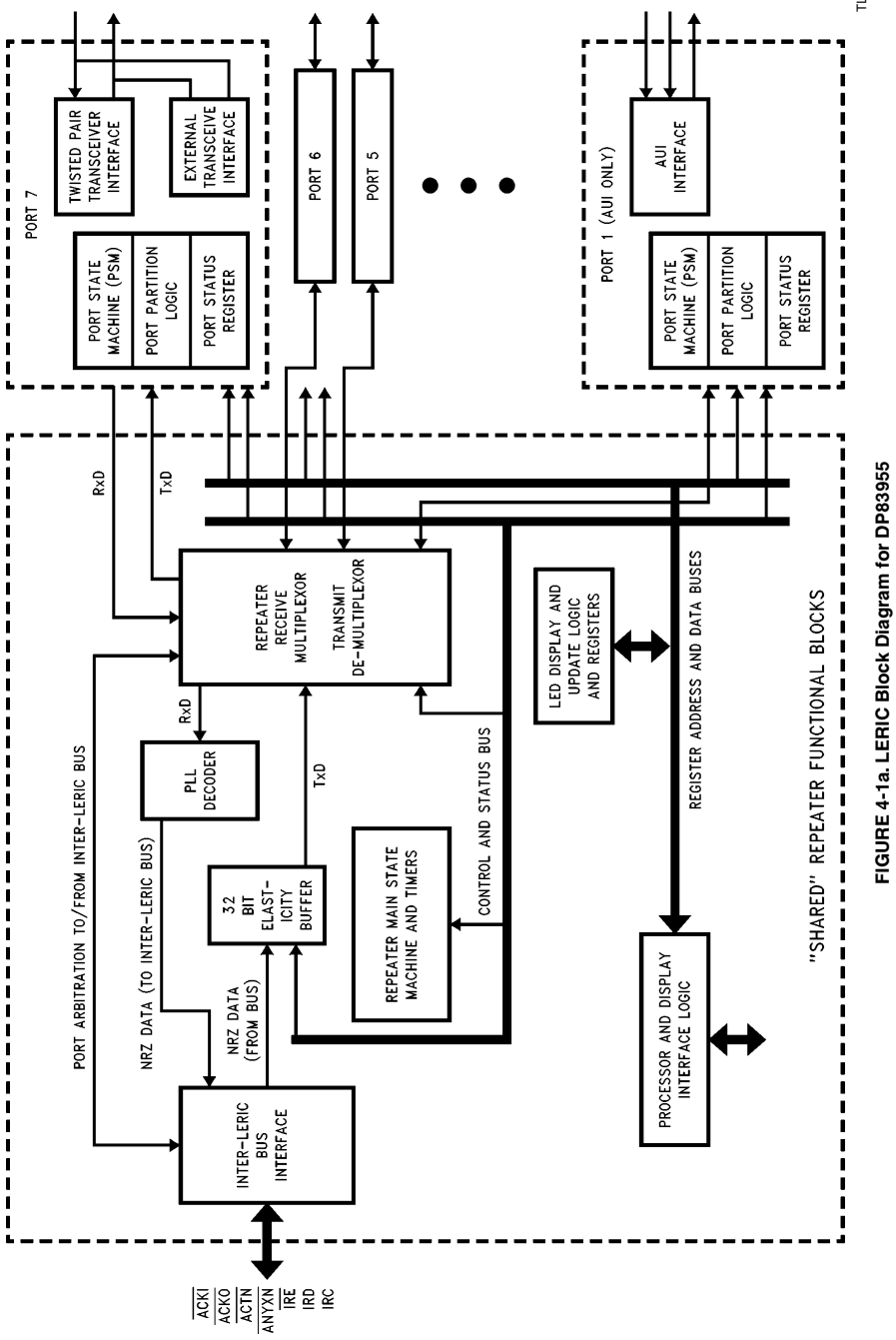


FIGURE 4-1a. LERIC Block Diagram for DP83955

4.0 Block Diagram (Continued)

4.0.2 DP83956 BLOCK DIAGRAM

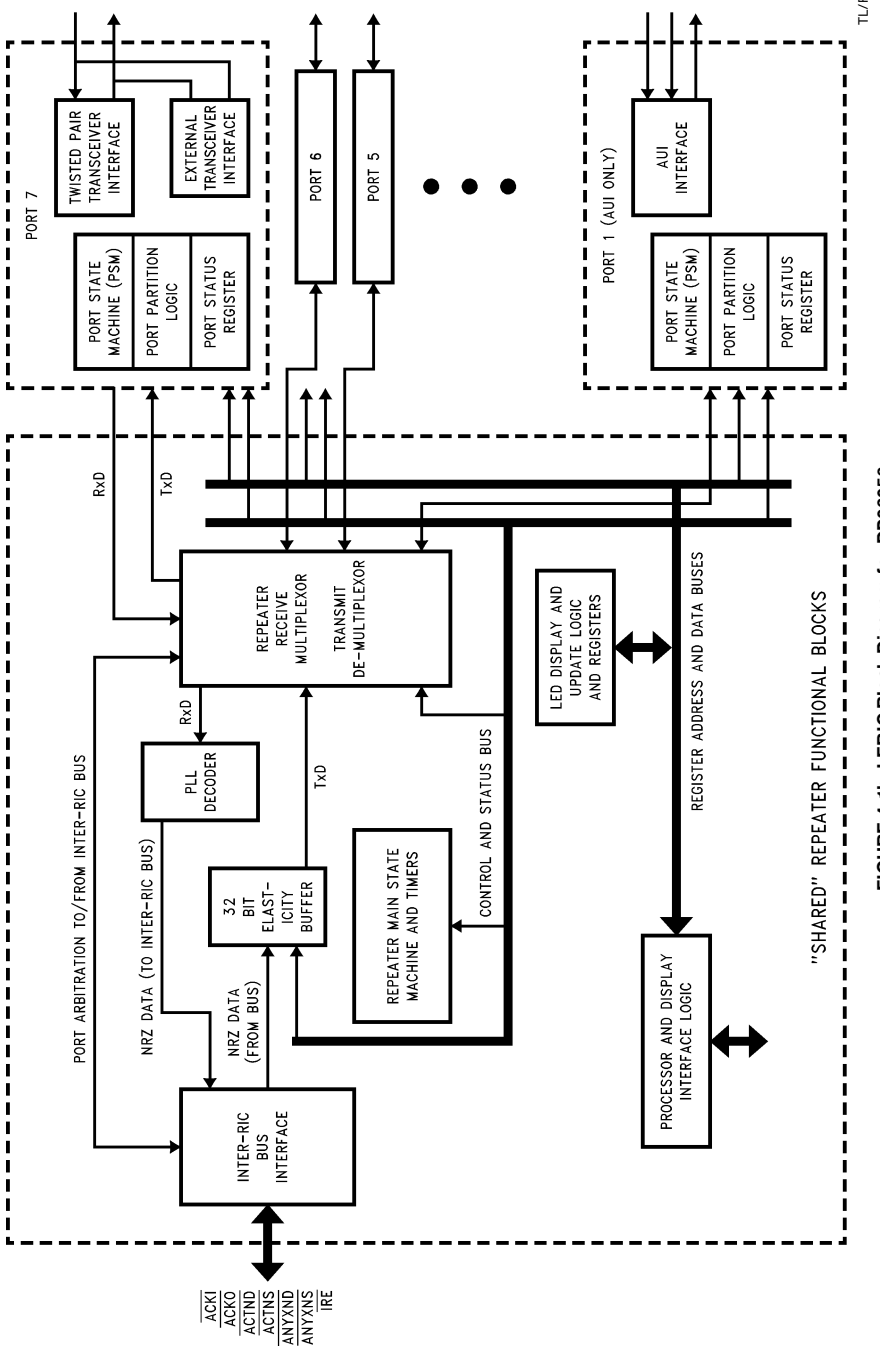


FIGURE 4-1b. LERIC Block Diagram for DP83956

5.0 Functional Description

The IEEE 802.3 repeater specification details a number of functions a repeater system must perform. These requirements allied with a need for the implementation to be multiport strongly favors the choice of a modular design style. In such a design, functionality is split between those tasks common to all data channels and those exclusive to each individual channel. The LERIC, much like the DP83950 RIC, follows this approach. Certain functional blocks are replicated for each network attachment (also known as a repeater port), and others are shared. The following section briefly describes the functional blocks in the LERIC.

5.1 OVERVIEW OF LERIC FUNCTIONS

Segment Specific Block: Network Port

As shown in the Block Diagram, the segment specific blocks consist of:

1. One or more physical layer interfaces.
2. A logic block required for performing repeater operations upon that particular segment. This is known as the ''port'' logic since it is the access ''port'' the segment has to the rest of the network.

This function is repeated 7 times in the LERIC (one for each port) and is shown on the right side of the Block Diagram, *Figure 4-1*.

The physical layer interfaces provided depends upon the port under examination. Port 1 has an AUI compliant interface for use with AUI compatible transceiver boxes and cable. Ports 2 to 7 may be configured for use with one of two interfaces: twisted pair or an external transceiver. The former utilizes the LERIC's on-chip 10BASE-T transceivers, the latter allows connection to external transceivers. When using the external transceiver mode the interface is AUI compatible. Although AUI compatible transceivers are supported the interface is not designed for use with an interface cable, thus the transceivers are necessarily internal to the repeater equipment.

Inside the port logic there are 3 distinct functions:

1. The port state machine (PSM) is required to perform data and collision repetition as described by the repeater specification, for example, it determines whether this port should be receiving from or transmitting to its network segment.
2. The port partition logic implements the segment partitioning algorithm. This algorithm is defined by the IEEE specification and is used to protect the network from malfunctioning segments.
3. The port status register reflects the current status of the port. It may be accessed by a system processor to obtain this status or to perform certain port configuration operations, such as port disable and squelch level selection.

Shared Functional Blocks: Repeater Core Logic

The shared functional blocks consist of the Repeater Main Status Machine (MSM) and Timers, a 32-bit Elasticity Buffer, PLL Decoder, and Receive and Transmit Multiplexers. These blocks perform the majority of the operations needed to fulfill the requirements of the IEEE repeater specification.

When a packet is received by a port, it is sent via the Receive Multiplexer to the PLL Decoder. Notification of the data and collision status is sent to the main state machine via the receive multiplexer and collision activity status signals. This enables the main state machine to determine the source of the data to be repeated and the type of data to be transmitted. The transmit data may be either the received packet's data field or a preamble/jam pattern consisting of a 1010 . . . bit pattern.

Associated with the main state machine are a series of timers. These ensure various IEEE specification times (referred to as the TW1 to TW6 times) are fulfilled.

A repeater unit is required to meet the same signal jitter performance as any receiving node attached to a network segment. Consequently, a phase locked loop Manchester decoder is required so that the packet may be decoded, and the jitter accumulated over the receiving segment eliminated. The decode logic outputs data in NRZ format with an associated clock and enable. In this form the packet is in a convenient format for transfer to other devices, such as network controllers and other LERICs, via the Inter-LERIC bus (described later). The data may then be re-encoded into Manchester data and transmitted.

Reception and transmission via physical layer transceiver units causes a loss of bits in the preamble field of a data packet. The repeater specification requires this loss to be compensated for. To accomplish this an elasticity buffer is employed to temporarily store bits in the data field of the packet.

The sequence of operation is as follows. Soon after the network segment receiving the data packet has been identified, the LERIC begins to transmit the packet preamble pattern (1010 . . .) onto the other network segments. While the preamble is being transmitted the Elasticity Buffer monitors the decoded received clock and data signals (this is done via the Inter-LERIC/Inter-RIC bus as described later). When the start of frame delimiter ''SFD'' is detected the received data stream is written into the elasticity buffer. Removal of data from the buffer for retransmission is not allowed until a valid length preamble pattern has been transmitted.

Inter-LERIC/Inter-RIC Bus Interface

The LERIC can be cascaded either to other LERICs or RICs to facilitate the design of large multiport repeaters. The split of functions already described allows data packets and collision status to be transferred between multiple LERICs, and at the same time the multiple LERICs still behave as a single logical repeater. Since all LERICs in a repeater system are identical and capable of performing any of the repetition operations, the failure of one LERIC will not cause the failure of the entire system. This is an important issue in large multiport repeaters.

DP83955's communicate via a specialized interface known as the Inter-LERIC bus. DP83956s can communicate with other DP83956s and/or DP83950s via the Inter-RIC bus. These allow the data packets to be transferred from the receiving LERIC to the other LERICs in the system. These LERICs then transmit the data stream to their segments. Just as important as data transfer is the notification of collisions occurring across the network. The Inter-LERIC/Inter-RIC bus has a set of status lines capable of conveying collision information between LERICs to ensure their main state machines operate in the appropriate manner.

LED Interface

Repeater systems usually possess optical displays indicating network activity and the status of specific repeater operations. The LERIC's display update block provides the system designer with a wide variety of indicators. The display

5.0 Functional Description (Continued)

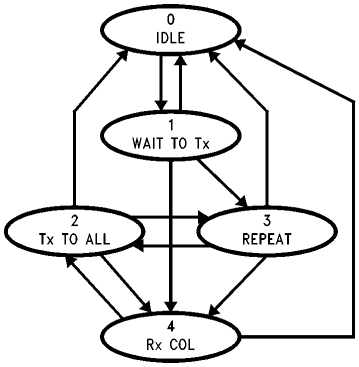
updates are completely autonomous and merely require SSI logic devices to drive the display devices, usually made up of light emitting diodes, LEDs. The status display is very flexible, allowing the user to choose those indicators appropriate for the specification of the equipment. The Display Frozen Strobe ($\overline{DFS}$) may be used to latch the various indicators which are frozen at the end of the activity. The LED display will be frozen for 30 ms after the end of the activity, or until a new activity has started, whichever is shorter. Note that the complete LED display cycle for all the ports takes approximately 1.6 μs.

Processor Interface

The LERIC's processor interface allows connection to a system processor (or a simple read/write logic interface). Data transfer occurs via a 4-bit bidirectional data bus, and 4-bit address bus. Display update cycles and processor accesses occur utilizing the same bus. An on-chip arbiter in the processor/display block schedules and controls the accesses and ensures the correct information is written into the display latches. During the display update cycles the LERIC behaves as a master of its bus. This is the default state of the bus. Consequently, a TRI-STATE buffer must be placed between the LERIC and the system processor's data bus. This ensures bus contention is avoided during simultaneous display update cycles and processor accesses of other devices on the system bus. When the processor accesses a LERIC register, the LERIC enables the data buffer and selects the operation, either input to or output from the data pins.

5.2 DESCRIPTION OF REPEATER OPERATIONS

In order to implement a multi-chip repeater system which behaves as though it were a single logical repeater, special consideration must be paid to the data path used in packet repetition. For example, where in the path are specific operations such as Manchester decoding and elasticity buffering performed. Also the system's state machines which utilize available network activity signals, must be able to accommodate the various packet repetition and collision scenarios detailed in the IEEE 802.3 repeater specification.



TL/F/11240–7

FIGURE 5-1. Inter-LERIC/Inter-RIC Bus State Diagram

The LERIC contains two types of interacting state machines. These are:

1. Port State Machines (PSMs). Every network attachment has its own PSM.
2. Main State Machine (MSM). This state machine controls the shared functional blocks as shown in the block diagram *Figure 4-1*.

Repeater Port and Main State Machines

These two state machines are described in the following sections. Reference is made to expressions used in the IEEE 802.3 Repeater specification. For the precise definition of these terms please refer to the IEEE specifications. To avoid confusion with the LERIC's implementation, where references are made to repeater states or terms as described in the IEEE specification, these items are written in *italics*. The IEEE state diagram is shown in *Figure 5-2*, the Inter-LERIC/Inter-RIC bus state diagram is shown in *Figure 5-1*.

5.0 Functional Description (Continued)

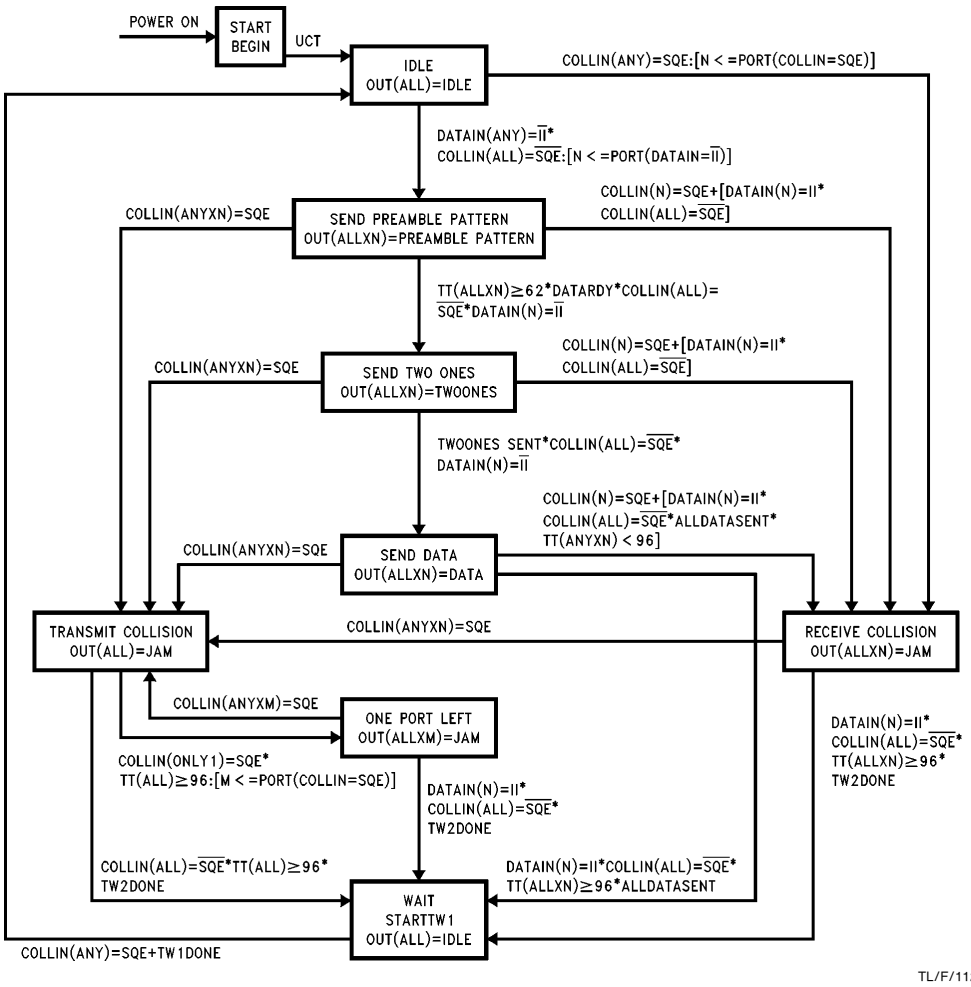


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FIGURE 5-2. IEEE Repeater Main State Diagram

5.0 Functional Description (Continued)

Port State Machine (PSM)

There are two primary functions for the PSM as follows:

1. Control the transmission of repeated data and jam signals over the attached segment.
2. Decide whether a port will be the source of data or collision information which will be repeated over the network. This repeater port is known as *PORT N*. An arbitration process is required to enable the repeater to transition from the *IDLE* state to the *SEND PREAMBLE PATTERN* or *RECEIVE COLLISION* states, see *Figure 5-2*. This process is used to locate the port which will be *PORT N* for that particular packet. The data received from this port is directed to the PLL decoder and transmitted over the Inter-LERIC bus. If the repeater enters the *TRANSMIT COLLISION* state a further arbitration operation is performed to determine which port is *PORT M*. *PORT M* is differentiated from the repeater's other ports if the repeater enters the *ONE PORT LEFT* state. In this state *PORT M* does not transmit to its segment; where as all other ports are still required to transmit to their segments.

Main State Machine (MSM)

The MSM controls the operation of the shared functional blocks in each LERIC as shown in the block diagram, *Figure 4-1*, and it performs the majority of the data and collision propagation operations as defined by the IEEE specification, these include those shown in Table 5-1.

The interaction of the main and port state machines is visible, in part, by observing the Inter-LERIC bus.

TABLE 5-1. Main State Machine Operations

Function	Action
Preamble Regeneration	Restore the length of the preamble pattern to the defined size.
Fragment Extension	Extend received data or collision fragments to meet the minimum fragment length of 96 bits.
Elasticity Buffer Control	A portion of the received packet may require storage in an Elasticity Buffer to accommodate preamble regeneration.
Jam/ Preamble Pattern Generation	In cases of receive or transmit collisions a LERIC is required to transmit a jam pattern (1010 . . .). **Note:** This pattern is the same as that used for preamble regeneration.
Transmit Collision Enforcement	Once the *TRANSMIT COLLISION* state is entered a repeater is required to stay in this state for at least 96 network bit times.
Data Encoding Control	NRZ format data from the elasticity buffer must be encoded into Manchester format data prior to retransmission.
Tw1 Enforcement	Enforce the Transmit Recovery Time specification.
Tw2 Enforcement	Enforce Carrier Recovery Time specification on all ports with active collisions.

Inter-LERIC Bus Operation

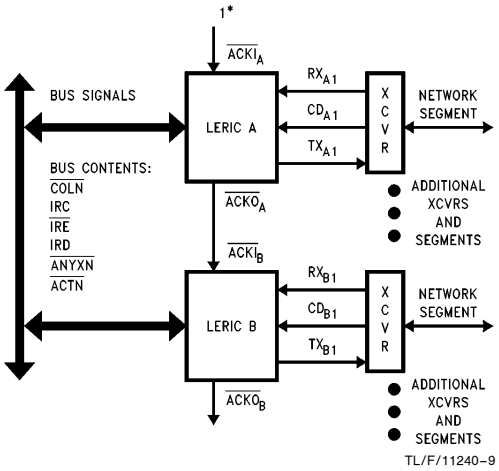
Overview

The Inter-LERIC Bus, like the Inter-RIC Bus, consists of eight signals. These signals implement a protocol which may be used to connect multiple LERICs together. In this configuration, the logical function of a single repeater is maintained. The resulting multi-LERIC system is compliant to the IEEE 802.3 Repeater Specification and may connect several hundred network segments. An example of a multi-LERIC system is shown in *Figure 5-3*.

The Inter-LERIC Bus connects multiple LERICs to realize the following operations:

Port N Identification (which port the repeater receives data from)
Port M Identification (which port is the last one experiencing a collision)
Data Transfer
RECEIVE COLLISION identification
TRANSMIT COLLISION identification
DISABLE OUTPUT (jabber protection)

The following tables briefly describe the operation of each bus signal, the conditions required for a LERIC to assert a signal and which LERICs (in a multi-LERIC system) would monitor a signal:



*__Note 1:__ This input is tied at a logic high state.

FIGURE 5-3. LERIC System Topology

5.0 Functional Description (Continued)

$\overline{\text{ACKI}}$

Function	Input signal to the PSM arbitration chain. This chain is employed to identify *PORT N* and *PORT M*. **Note:** A LERIC which contains *PORT N* or *PORT M* may be identified by its $\overline{\text{ACKO}}$ signal being low when its $\overline{\text{ACKI}}$ input is high.
Conditions required for a LERIC to drive this signal	Not Applicable
LERIC Receiving the Signal	This is dependent upon the method used to cascade LERICs, described in Section 5.3.

$\overline{\text{ACKO}}$

Function	Output signal from the PSM arbitration chain.
Conditions required for a LERIC to drive this signal	This is dependent upon the method used to cascade LERICs, described in Section 5.3.
LERIC Receiving the Signal	Not Applicable

$\overline{\text{ACTN}}$

Function	This signal denotes there is activity on *PORT N* or *PORT M*.
Conditions required for a LERIC to drive this signal	A LERIC must contain *PORT N* or *PORT M*. **Note:** Although this signal normally has only one source asserting the signal active it is used in a wired-OR configuration.
LERIC Receiving the Signal	The signal is monitored by all LERICs in the repeater system.

$\overline{\text{ANYXN}}$

Function	This signal denotes that a repeater port that is not *Port N* or *Port M* is experiencing a collision.
Conditions required for a LERIC to drive this signal	Any LERIC which satisifies the above condition. **Note:** This bus line is used in a wired-OR configuration.
LERIC Receiving the Signal	The signal is monitored by all LERICs in the repeater system.

$\overline{\text{COLN}}$

Function	Denotes *PORT N* or *PORT M* is experiencing a collision.
Conditions required for a LERIC to drive this signal	A LERIC must contain *PORT N* or *PORT M*.
LERIC Receiving the Signal	The Signal is monitored by all other LERICs in the repeater system.

$\overline{\text{IRE}}$

Function	This signal acts as an activity framing signal for the IRC and IRD signals.
Conditions required for a LERIC to drive this signal	A LERIC must contain *PORT N*.
LERIC Receiving the Signal	The Signal is monitored by all other LERICs in the repeater system.

IRD

Function	Decoded serial data, in NRZ format, received from the network segment attached to *PORT N*.
Conditions required for a LERIC to drive this signal	A LERIC must contain *PORT N*.
LERIC Receiving the Signal	The signal is monitored by all other LERICs in the repeater system.

IRC

Function	Clock signal associated with IRD and $\overline{\text{IRE}}$.
Conditions required for a LERIC to drive this signal	A LERIC must contain *PORT N*.
LERIC Receiving the Signal	The signal is monitored by all other LERICs in the repeater system.

5.0 Functional Description (Continued)

Methods of LERIC Cascading

In order to build multi-LERIC repeaters, *PORT N* and *PORT M* identification must be performed across all the LERICs in the system. Inside each LERIC the PSMs are arranged in a logical arbitration chain where Port 1 is the highest and Port 7 the lowest.

The top of the chain, the input to Port 1 is accessible to the user via the LERIC's $\overline{\text{ACKI}}$ input pin. The output from the bottom of the chain becomes the $\overline{\text{ACKO}}$ output pin. In a single LERIC system *PORT N* is defined as the highest port in the arbitration chain with receive or collision activity. *PORT N* identification is performed when the repeater is in the *IDLE* state. *PORT M* is defined as the highest port in the chain with a collision when the repeater leaves the *TRANSMIT COLLISION* state. In order for the arbitration chain to function, all that needs to be done is to tie the $\overline{\text{ACKI}}$ signal to a logic high state. In multi-LERIC systems there are two methods to propagate the arbitration chain between LERICs:

The first and most straightforward way is to extend the arbitration chain by daisy-chaining the $\overline{\text{ACKI}}$–$\overline{\text{ACKO}}$ signals between LERICs. In this approach one LERIC is placed at the top of the chain (its $\overline{\text{ACKI}}$ input is tied high), then the $\overline{\text{ACKO}}$ signal from this LERIC is sent to the $\overline{\text{ACKI}}$ input of the next LERIC and so on. This arrangement is simple to implement but it places some topological restrictions upon the repeater system. In particular, when the repeater is constructed using a backplane with removable printed circuit boards containing the LERICs, if one of the boards is removed then the $\overline{\text{ACKI}}$–$\overline{\text{ACKO}}$ chain will be broken and the repeater will not operate correctly.

The second method of *PORT N* or *M* identification avoids this problem. This second technique relies on an external parallel arbiter which monitors all of the LERICs' $\overline{\text{ACKO}}$ signals and responds to the LERIC with the highest priority. In this scheme each LERIC is assigned with a priority level. One method of doing this is to assign a priority number which reflects the position of a LERIC board on the repeater backplane (i.e., its slot number). When a LERIC experiences receive activity and the repeater system is in the *IDLE* state, the LERIC board will assert $\overline{\text{ACKO}}$. External arbitration logic drives the identification number onto an arbitration bus and the LERIC containing *PORT N* will be identified. An identical procedure is used in the *TRANSMIT COLLISION* state to identify *PORT M*. This parallel means of arbitration is not subject to the problems caused by missing boards (i.e., empty slots in the backplane). The logic associated with asserting this arbitration vector in the various packet repetition scenarios could be implemented in PAL® or GAL® type devices.

To perform *PORT N* or *M* arbitration, both of the above methods employ the same signals: $\overline{\text{ACKI}}$, $\overline{\text{ACKO}}$, and $\overline{\text{ACTN}}$.

The Inter-LERIC bus allows multi-LERIC operations to be performed in exactly the same manner as if there is only a single LERIC in the system. The simplest way to describe the operation of Inter-LERIC bus is to see how it is used in a number of common packet repetition scenarios. Throughout this description the LERICs are presumed to be operating in external transceiver mode. This is advantageous for the explanation since the receive, transmit and collision signals from each network segment are observable. In internal transceiver mode this is not the case, since the collision signal for the non-AUI ports is derived by the transceivers inside the LERIC.

5.3 EXAMPLES OF PACKET REPETITION SCENARIOS

Data Repetition

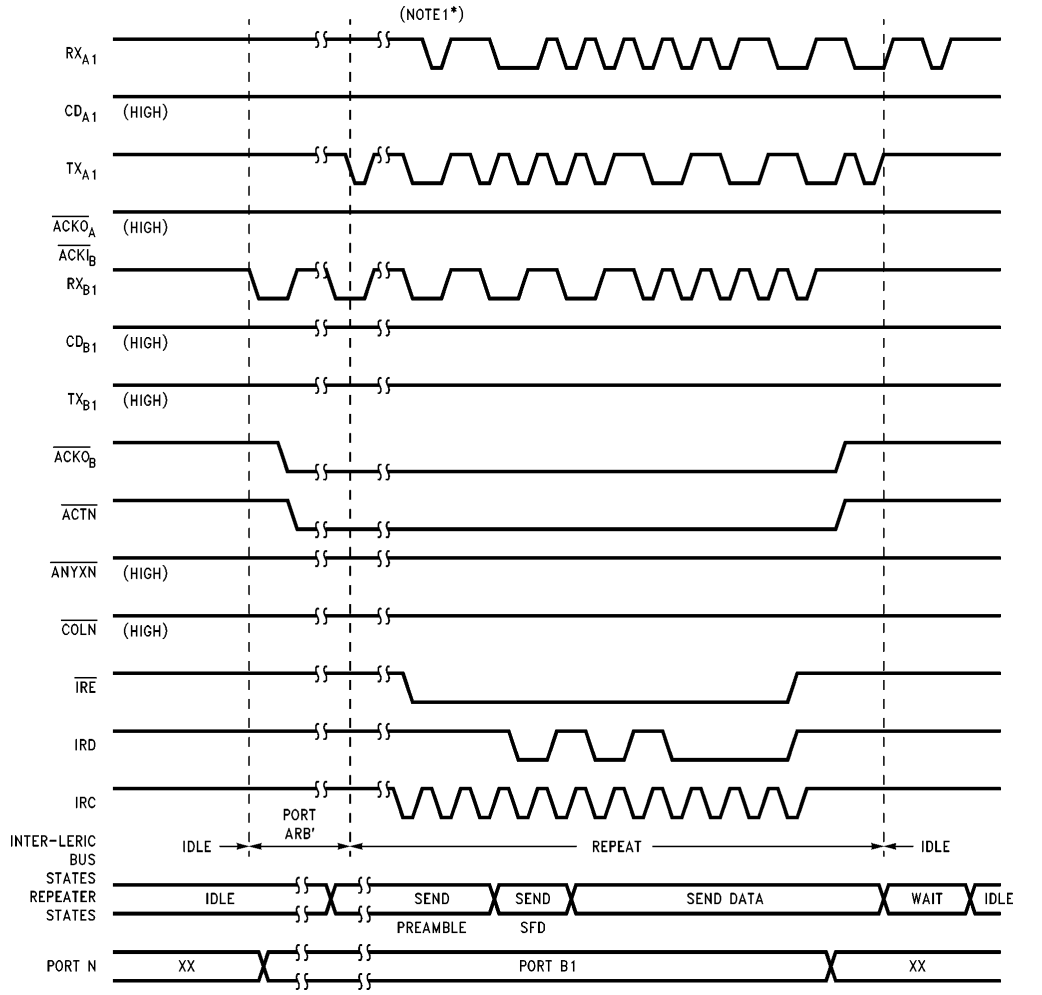
The simplest packet operation performed over the Inter-LERIC Bus is data repetition. In this operation a data packet is received at one port and transmitted to all other segments.

The first task to be performed is *PORT N* identification. This is an arbitration process performed by the Port State Machines in the system. In situations where two or more ports simultaneously receive packets the Inter-LERIC bus operates by choosing one of the active ports and forcing the others to transmit data. This is done to faithfully follow the IEEE specification's allowed exit paths from the *IDLE* state (i.e., to the *SEND PREAMBLE PATTERN* or *RECEIVE COLLISION* states).

The packet begins with a preamble pattern derived from the LERIC's on chip jam/preamble generator. The data received at *PORT N* is directed through the receive multiplexer to the PLL decoder. Once phase lock has been achieved, the decoded data, in NRZ format, with its associated clock and enable signals are asserted onto the IRD, $\overline{\text{IRE}}$ and IRC Inter-LERIC bus lines. This serial data stream is received from the bus by all LERICs in the repeater and directed to their Elasticity Buffers. Logic circuits monitor the data stream and look for the Start of Frame Delimiter (SFD). When this has been detected data is loaded into the elasticity buffer for later transmission. This will occur when sufficient preamble has been transmitted and certain internal state machine operations have been fulfilled.

Figure 5-3 shows two LERICs, A and B, daisy-chained together with LERIC A positioned at the top of the chain. A packet is received at port B1 of LERIC B and is then repeated by the other ports in the system. *Figure 5-4* shows the functional timing diagram for this packet repetition represented by the signals shown in *Figure 5-3*. In this example only two ports in the system are shown, obviously the other ports also repeat the packet. It also indicates the operation of the LERICs' state machines in so far as can be seen by observing the Inter-LERIC bus. For reference, the repeater's state transitions are shown in terms of the states defined by the IEEE specification. The location (i.e., which port it is) of *PORT N* is also shown. The following section describes the repeater and Inter-LERIC bus transitions shown in *Figure 5-4*.

5.0 Functional Description (Continued)



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*__Note 1:__ The activity shown on RX_{A1} represents the transmitted signal on TX_{A1} after being looped back by the attached transceiver.

FIGURE 5-4. Data Repetition

5.0 Functional Description (Continued)

The repeater is stimulated into activity by the data signal received by port B1. The LERICs in the system are alerted to forthcoming repeater operation by the falling edges on the $\overline{ACKI}$–$\overline{ACKO}$ daisy chain and the $\overline{ACTN}$ bus signal. Following a defined start up delay the repeater moves to the *SEND PREAMBLE* state. The LERIC system utilizes the start up delay to perform port arbitration. When packet transmission begins the LERIC system enters the REPEAT state. The expected, for normal packet repetition, sequence of repeater states, *SEND PREAMBLE*, *SEND SFD* and *SEND DATA* is followed but is not visible upon the Inter-LERIC bus. They are merged together into a single REPEAT state. This is also true for the *WAIT* and *IDLE* states, they appear as a combined Inter-LERIC bus IDLE state.

Once a repeat operation has begun (i.e., the repeater leaves the *IDLE* state) it is required to transmit at least 96 bits of data or jam/preamble onto its network segments. If the duration of the received signal from *PORT N* is smaller than 96 bits, the repeater transitions to the *RECEIVE COLLISION* state (described later). This behavior is known as fragment extension.

After the packet data has been repeated, including the emptying of the LERICs' elasticity buffers, the LERIC performs the *Tw1* transmit recovery operation. This is performed during the *WAIT* state shown in the repeater state diagram.

Receive Collisions

A receive collision is a collision which occurs on the network segment attached to *PORT N* (i.e., the collision is ''received'' in a similar manner as a data packet is received and then repeated to the other network segments). Not surprisingly, receive collision propagation follows a similar sequence of operations as is found with data repetition:

An arbitration process is performed to find *PORT N* and a preamble/jam pattern is transmitted by the repeater's other ports. When *PORT N* detects a collision on its segment the $\overline{COLN}$ Inter-LERIC bus signal is asserted. This forces all the LERICs in the system to transmit a preamble/jam pattern to their segments. This is important since they may be already transmitting data from their elasticity buffers. The repeater moves to the *RECEIVE COLLISION* state when the LERICs begin to transmit the jam pattern. The repeater remains in this state until both the following conditions have been fulfilled:

1. At least 96 bits have been transmitted onto the network,
2. The activity has ended.

Under close examination the repeater specification reveals that the actual end of activity has its own permutations of conditions:

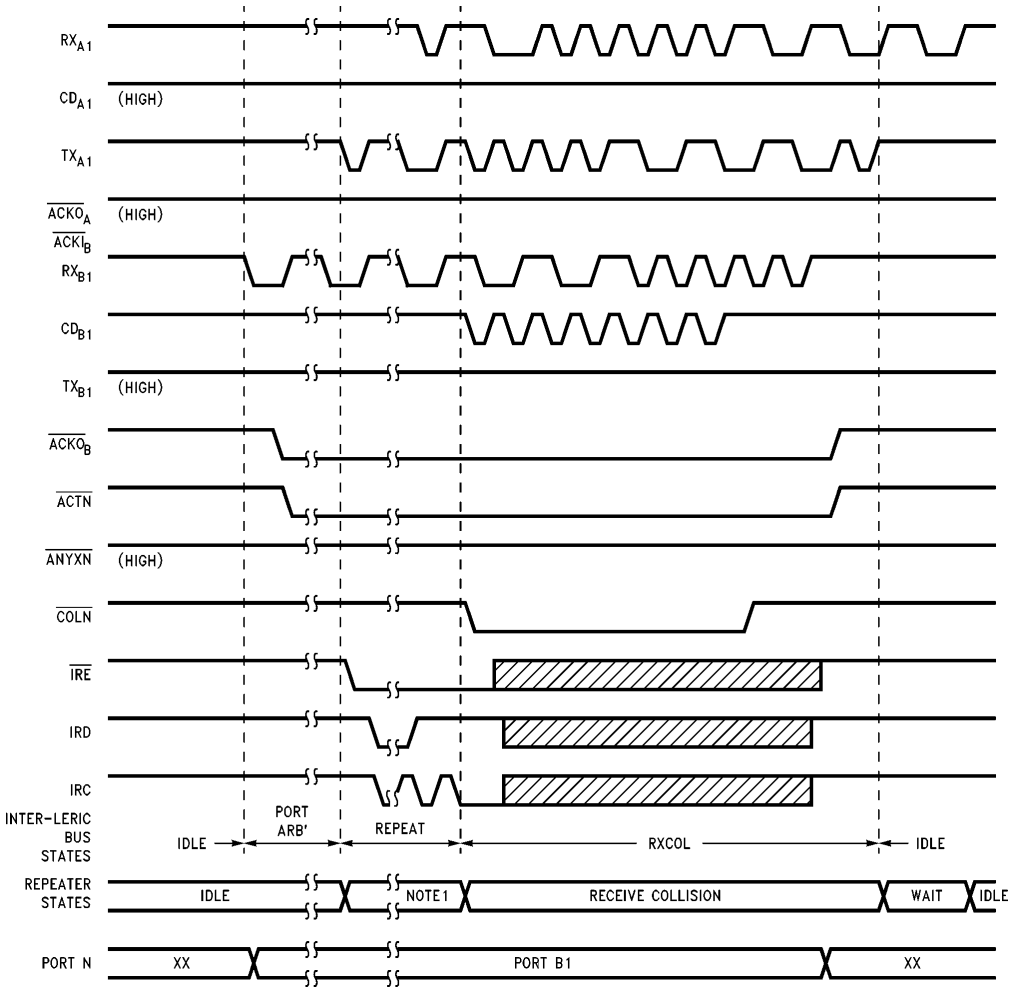
1. Collision and receive data signals may end simultaneously,
2. Receive data may appear to end before collision signals,
3. Receive data may continue for some time after the end of the collision signal.

Network segments using coaxial media may experience spurious gaps in segment activity when the collision signal goes inactive. This arises from the inter-action between the receive and collision signal squelch circuits, implemented in coaxial transceivers, and the properties of the coaxial cable itself. The repeater specification avoids propagation of these activity gaps by extending collision activity by the *Tw2* wait time. Jam pattern transmission must be sustained throughout this period. After this, the repeater will move to the *WAIT* state unless there is a data signal being received by *PORT N*.

The functional timing diagram, *Figure 5-5,* shows the operation of a repeater system during a receive collision. The system configuration is the same as earlier described and is shown in *Figure 5-3*.

The LERICs perform the same *PORT N* arbitration and data repetition operations as previously described. The system is notified of the receive collision on port B1 by the $\overline{COLN}$ bus signal going active. This is the signal which informs the main state machines to output the jam pattern rather than the data held in the elasticity buffers. Once a collision has occurred the IRC, IRD and $\overline{IRE}$ bus signals may become undefined. When the collision has ended and the *Tw2* operation performed, the repeater moves to the *WAIT* state.

5.0 Functional Description (Continued)



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*__Note 1:__ *SEND PREAMBLE, SEND SFD, SEND DATA*

FIGURE 5-5. Receive Collision

5.0 Functional Description (Continued)

Transmit Collisions

A transmit collision is a collision that is detected upon a segment to which the repeater system is transmitting. The port state machine monitoring the colliding segment asserts the $\overline{\text{ANYXN}}$ bus signal. The assertion of $\overline{\text{ANYXN}}$ causes *PORT M* arbitration to begin. The repeater moves to the *TRANSMIT COLLISION* state when the port which had been *PORT N* starts to transmit a Manchester encoded 1 on to its network segment. While in the *TRANSMIT COLLISION* state all ports of the repeater must transmit the 1010 . . . jam pattern and *PORT M* arbitration is performed. Each LERIC is obliged, by the IEEE specification, to ensure all of its ports transmit for at least 96 bits once the *TRANSMIT COLLISION* state has been entered. This transmit activity is enforced by the $\overline{\text{ANYXN}}$ bus signal. While $\overline{\text{ANYXN}}$ is active all LERIC ports will transmit jam. To ensure this situation lasts for at least 96 bits, the MSMs inside the LERICs assert the $\overline{\text{ANYXN}}$ signal throughout this period. After this period has elapsed, $\overline{\text{ANYXN}}$ will only be asserted if there are multiple ports with active collisions on their network segments.

There are two posible ways for a repeater to leave the *TRANSMIT COLLISION* state. The most straightforward is when network activity (i.e., collisions and their *Tw2* extensions) end before the 96-bit enforced period expires. Under these conditions the repeater system may move directly to the *WAIT* state when 96 bits have been transmitted to all ports. If the MSM enforced period ends and there is still one port experiencing a collision the *ONE PORT LEFT* state is entered. This may be seen on the Inter-LERIC bus when $\overline{\text{ANYXN}}$ is deasserted and *PORT M* stops transmitting to its network segment. In this circumstance the Inter-LERIC bus transitions to the RECEIVE COLLISION state. The repeater will remain in this state while *PORT M's* collision, *Tw2* collision extension and any receive signals are present. When these conditions are not true, packet repetition finishes and the repeater enters the *WAIT* state.

Figure 5-6 shows a multi-LERIC system operating under transmit collision conditions. There are many different scenarios which may occur during a transmit collision, this figure illustrates one of these. The diagram begins with packet reception by port A1. Port B1 experiences a collision, since it is not *PORT N* it asserts $\overline{\text{ANYXN}}$. This alerts the main state machines in the system to switch from data to jam pattern transmission.

Port A1 is also monitoring the $\overline{\text{ANYXN}}$ bus line. Its assertion forces A1 to relinquish its *PORT N* status, start transmitting, stop asserting $\overline{\text{ACTN}}$ and release its hold on the PSM arbitration signals ($\overline{\text{ACKO}}$ A and $\overline{\text{ACKI}}$ B). The first bit it transmits will be a Manchester encoded ''1'' in the jam pattern. Since port B1 is the only port with a collision, it attains *PORT M* status and stops asserting $\overline{\text{ANYXN}}$. It does however assert $\overline{\text{ACTN}}$, and exert its presence upon the PSM arbitration chain (forces $\overline{\text{ACKO}}$ B low). The MSMs ensure that $\overline{\text{ANYXN}}$ stays active and thus forces all of the ports, including *PORT M*, to transmit to their segments.

After some time port A1 experiences a collision. This arises from the presence of the packet being received from port A1's segment plus the jam signal the repeater is now transmitting onto this segment. Two packets on one segment results in a collision. *PORT M* now moves from B1 to A1. Port A1 fulfills the same criteria as B1 (i.e., it has an active collision on its segment), but in addition it is higher in the arbitration chain. This priority yields no benefits for port A1 since the $\overline{\text{ANYXN}}$ signal is still active. There are now two sources driving $\overline{\text{ANYXN}}$, the MSMs and the collision on port B1.

Eventually the collision on port B1 ends and the $\overline{\text{ANYXN}}$ extension by the MSMs expires. There is only one collision on the network (this may be deduced since $\overline{\text{ANYXN}}$ is inactive) so the repeater will move to the *ONE PORT LEFT* state. The LERIC system treats this state in a similar manner to a receive collision with *PORT M* fulfilling the role of the receiving port. The difference from a true receive collision is that the switch from packet data to the jam pattern has already been made (controlled by $\overline{\text{ANYXN}}$). Thus the state of $\overline{\text{COLN}}$ has no effect upon repeater operations. In common with the operation of the *RECEIVE COLLISION* state, the repeater remains in this condition until the collision and receive activity on *PORT M* subside. The packet repetition operation completes when the *Tw1* recovery time in the *WAIT* state has been performed.

Note: In transmit collision conditions $\overline{\text{COLN}}$ will only go active if the LERIC which contained *PORT N* at the start of packet repetition contains *PORT M* during the *TRANSMIT COLLISION* and *ONE PORT LEFT* states.

5.0 Functional Description (Continued)

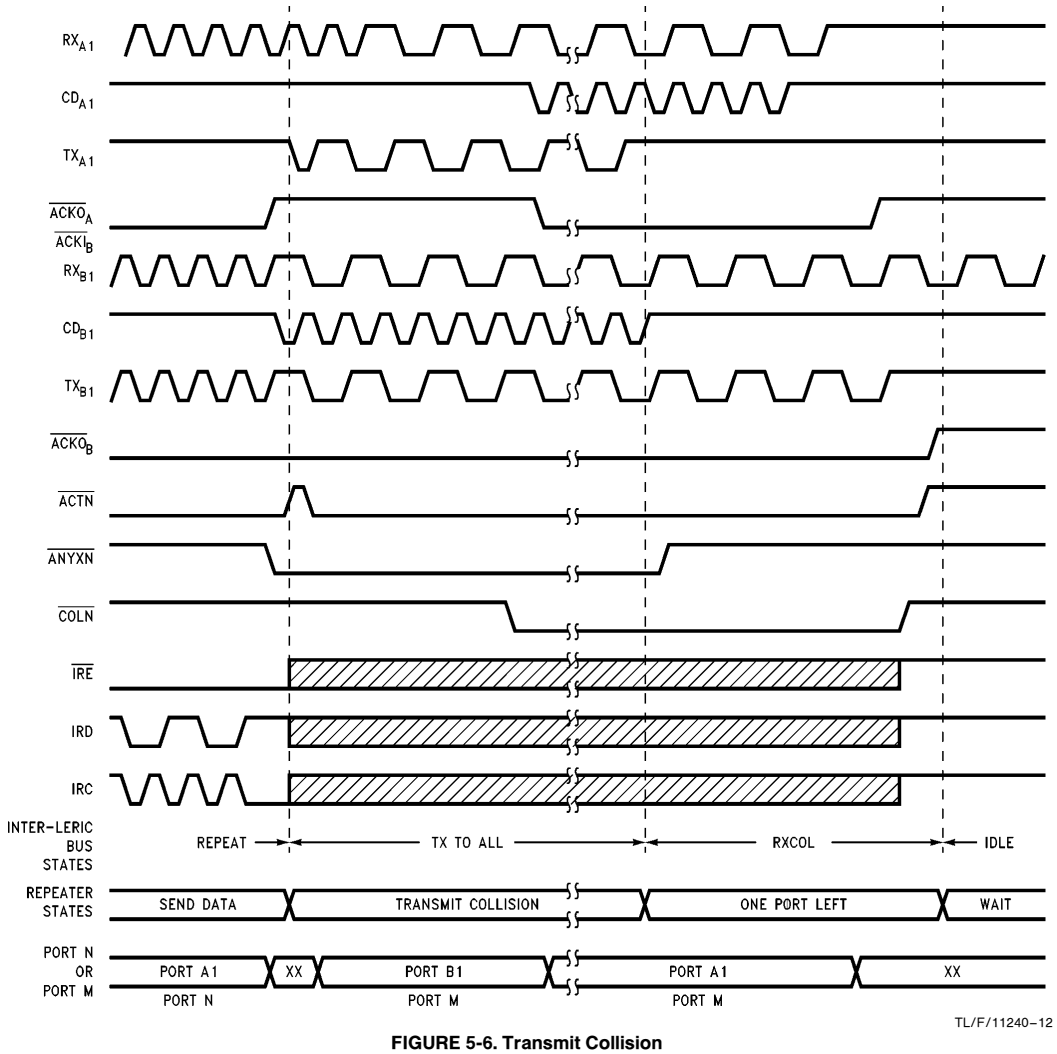

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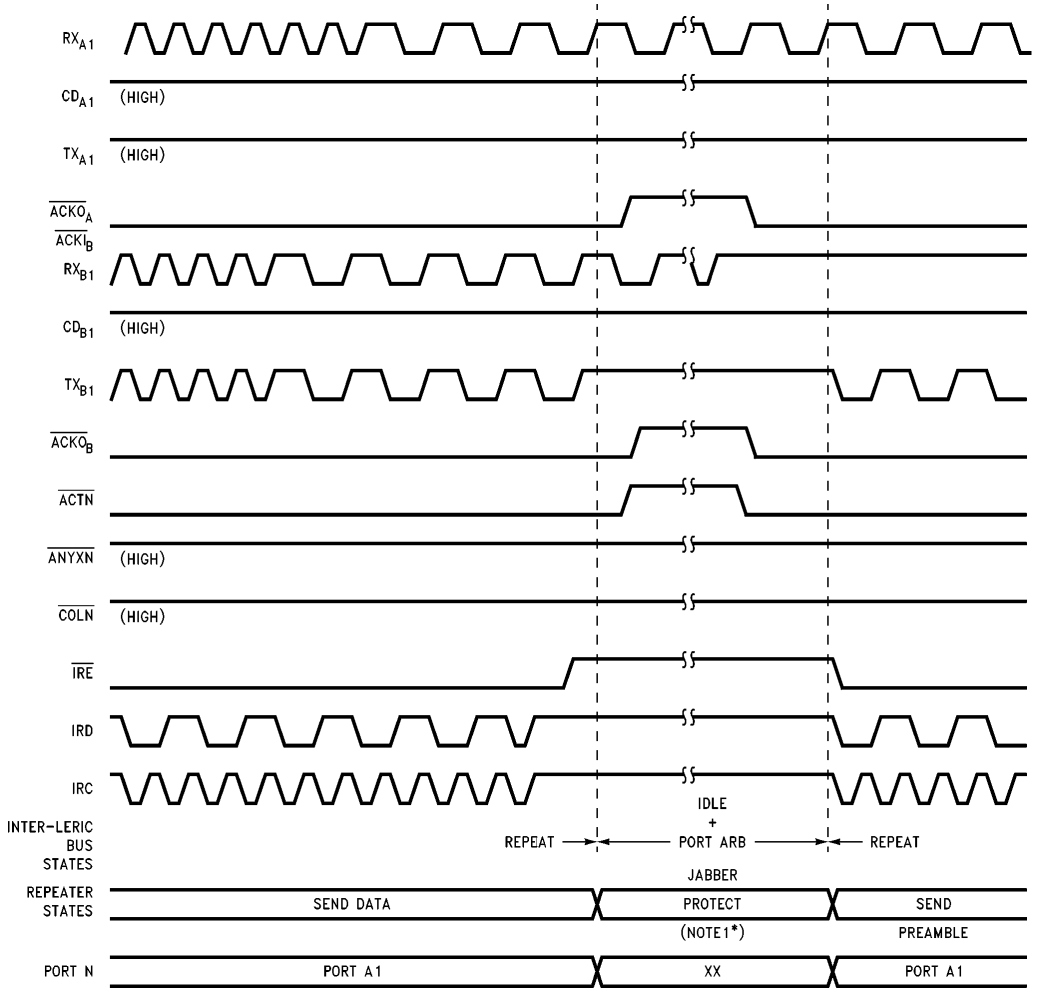
FIGURE 5-6. Transmit Collision

5.0 Functional Description (Continued)

Jabber Protection

A repeater is required to disable transmit activity if the length of its current transmission reaches the jabber protect limit. This is defined by the IEEE specification's *Tw3* time. The repeater disables output for a time period defined by the *Tw4* specification, after this period normal operation may resume.

Figure 5-7 shows the effect of a jabber length packet upon a LERIC based repeater system. The **JABBER PROTECT** state is entered from the *SEND DATA* state. While the *Tw4* period is observed the Inter-LERIC bus displays the IDLE state. This is misleading since new packet activity or continuous activity (as shown in the diagram) does not result in packet repetition. This may only occur when the *Tw4* requirement has been satisfied.



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***Note 1:** The IEEE Specification does not have a jabber protect state defined in its main state diagram, this behavior is defined in an additional MAU Jabber Lockup Protection state diagram.

FIGURE 5-7. Jabber Protect

5.0 Functional Description (Continued)

5.4 DESCRIPTION OF HARDWARE CONNECTION FOR CASCADING

5.4.1 DP89355 on the Inter-LERIC Bus

When considering the hardware interface the Inter-LERIC bus may be viewed as consisting of three groups of signals:

1. Port Arbitration chain, namely: $\overline{\text{ACKI}}$ and $\overline{\text{ACKO}}$. These signals are either used as point-to-point links or with external arbitration logic. In both cases the load on these signals will not be large so that the on-chip drivers are adequate.
2. Simultaneous drive and sense signals, namely: $\overline{\text{ACTN}}$ and $\overline{\text{ANYXN}}$. Potentially these signals may be driven by multiple devices. It should be noticed that due to the nature of these signals, transceivers cannot be implemented for the purpose of cascading; however, bench evaluation indicates that LERICs can be cascaded together as long as the total load capacitance is 100 pF or less.
3. Drive or sense signals (i.e., $\overline{\text{IRE}}$, IRD, IRC and $\overline{\text{COLN}}$). Only one device asserts these signals at any instance in time. The unidirectional nature of information transfer on the $\overline{\text{IRE}}$, IRD, IRC and $\overline{\text{COLN}}$ signals means a LERIC is either driving these signals or receiving them from the bus but not both at the same time. Thus a single bidirectional input/output pin is adequate for each of these signals.

5.4.2 DP83956 Using the Inter-RIC Bus

When considering the hardware interface the Inter-LERIC bus may be viewed as consisting of three groups of signals:

1. Port Arbitration chain, namely: $\overline{\text{ACKI}}$ and $\overline{\text{ACKO}}$. These signals are either used as point to point links or with external arbitration logic. In both cases the load on these signals will not be large so that the on-chip drivers are adequate.
2. The need for simultaneous sense and drive capabilities on the ACTN and ANYXN signals and the *desire to allow operation with external bus transceivers* makes it necessary for these bus signals to each have a pair of pins, one to drive the bus and the other to sense the bus. The Inter-LERIC bus on the DP83956 has been designed to connect LERICs together directly or via external bus transceivers. The latter is advantageous in large repeaters. When external bus transceivers are used they must be open collector/open drain to allow wire-ORing of the signals.
3. Drive or sense signals, i.e., $\overline{\text{IRE}}$, IRD, IRC and $\overline{\text{COLN}}$. Only one device asserts these signals at any instance in time. The unidirectional nature of information transfer on the $\overline{\text{IRE}}$, IRD, IRC and $\overline{\text{COLN}}$ signals means a LERIC is either driving these signals or receiving them from the bus but not both at the same time. Thus a single bidirectional input/output pin is adequate for each of these signals. When an external bus transceiver is used with these signals, the Packet Enable ''PKEN'', an output pin of LERIC, performs the function of a drive enable and sense disable.

5.5 PROCESSOR AND DISPLAY INTERFACE

The processor interface pins, which include the data bus, address bus and control signals, actually perform three operations which are multiplexed on these pins. These operations are:

1. The MLOAD Operation, which performs a power up initialization cycle upon the LERIC.
2. Display Update Cycles, which are refresh operations for updating the display LEDs.
3. Processor Access Cycles, which allow μP's (or simple logic) to communicate with the LERIC's registers.

These three operations are described below.

MLOAD Operation

The MLOAD Operation is a hardware initialization procedure performed at power on. It loads vital device configuration information into on chip configuration registers. In addition to its configuration function the $\overline{\text{MLOAD}}$ pin is the LERIC's reset input. When $\overline{\text{MLOAD}}$ is low all of the LERIC's repeater timers, state machines and segment partition logic are reset.

The MLOAD Operation may be accomplished by attaching the appropriate set of pull up and pull down resistors to the data and register address pins to assert logic high or low signals onto these pins, and then providing a rising edge on the $\overline{\text{MLOAD}}$ pin as is shown in *Figure 5-8.* The mapping of chip functions to the configuration inputs is shown in Table 5-2. Such an arrangement may be performed using a simple resistor, capacitor, diode network. Performing the MLOAD Operation in this way enables the configuration of a LERIC that is in a simple repeater system (one without a processor).

Alternatively, in a complex repeater system the MLOAD Operation may be performed using a processor write cycle. This would require the $\overline{\text{MLOAD}}$ pin be connected to the CPU's write strobe via some decoding logic, and included in the processor's memory map.

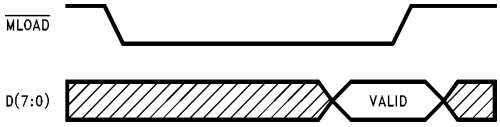

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FIGURE 5-8. MLOAD Operation

TABLE 5-2. Pin Definitions for Options in the MLOAD Operation

<table>
<tr><th>Pin Name</th><th>Programming Function</th><th>Effect When Bit is 0</th><th>Effect When Bit is 1</th><th>Function</th></tr>
<tr><td>D0
D1</td><td>BYPAS1
BYPAS2</td><td></td><td></td><td>
<table>
<tr><th>BYPAS2</th><th>BYPAS1</th><th>Information</th></tr>
<tr><td>0</td><td>0</td><td>All ports (2 to 7) use the external Transceiver Interface.</td></tr>
<tr><td>0</td><td>1</td><td>Ports 2 and 3 use the external interface, 4 to 7 use the internal 10BASE-T transceivers.</td></tr>
<tr><td>1</td><td>0</td><td>Ports 2 to 5 use the external interface, 6 and 7 use the internal 10BASE-T transceivers.</td></tr>
<tr><td>1</td><td>1</td><td>All ports (2 to 7) use the internal 10BASE-T transceivers.</td></tr>
</table>
These configuration bits select which of the repeater ports (numbers 2 to 7) are configured to use the on-chip internal 10BASE-T transceivers or the external transceiver interface. The external transceiver interface operates using AUI compatible signal levels.</td></tr>
<tr><td>D2</td><td>Resv.</td><td>Not Permitted</td><td>Required</td><td></td></tr>
<tr><td>D3</td><td>EPOLSW</td><td>Not Selected</td><td>Selected</td><td>Enables the polarity switching of the receive squelch upon detection of polarity reversal of the incoming data.</td></tr>
<tr><td>D4</td><td>Resv.</td><td>Not Permitted</td><td>Required</td><td></td></tr>
<tr><td>D5</td><td>$\overline{\text{TXONLY}}$</td><td>Selected</td><td>Not Selected</td><td>This configuration bit allows the on-chip partition algorithm to restrict segment reconnection, as described in the Partition State Machine.</td></tr>
<tr><td>D6</td><td>$\overline{\text{CCLIM}}$</td><td>63</td><td>31</td><td>The partition specification requires a port to be partitioned after a certain number of consecutive collisions. The LERIC has two values available to allow users to customize the partitioning algorithm to their environment. Please refer to the Partition State Machine, in data sheet section 7.3.</td></tr>
<tr><td>D7</td><td>MIN/MAX</td><td>Minimum Mode</td><td>Maximum Mode</td><td>The operation of the display update block is controlled by the value of this configuration bit, as described in the Display Update Cycles section.</td></tr>
</table>

5.0 Functional Description (Continued)

5.6 PROCESSOR AND DISPLAY INTERFACE HARDWARE CONNECTION

Display Update Cycles

The LERIC possesses control logic and interface pins which may be used to provide status information concerning activity on the attached network segments and the current status of repeater functions. These status cycles are completely autonomous and require only simple support circuitry to produce the data in a form suitable for a light emitting diode ''LED'' display. The display may be used in one of two modes:

1. Minimum Mode—General Repeater Status LEDs
2. Maximum Mode—Individual Port Status LEDs

Minimum mode, intended for simple LED displays, makes available four status indicators. The first LED denotes whether the LERIC has been forced to activate its jabber protect functions. The remaining 3 LEDs indicate if any of the LERIC's network segments are: (1) experiencing a collision, (2) receiving data, (3) currently partitioned. When minimum display mode is selected the only external components required are a 74LS374 type latch, the LEDs and their current limiting resistors.

Maximum mode differs from minimum mode by providing display information specific to individual network segments. This information denotes the collision activity, packet reception and partition status of each segment. In the case of 10BASE-T segments the link integrity status and polarity of the received data are also made available. The wide variety of information available in maximum mode may be used in its entirety or in part, thus allowing the system designer to choose the appropriate complexity of status display commensurate with the specification of the end equipment.

The signals provided and their timing relationships have been designed to interface directly with 74LS259 type addressable latches. The number of latches used being dependent upon the complexity of the display. Since the latches are octal, a pair of latches is needed to display each type of segment specific data (7 ports means 7 latch bits). The accompanying Tables 5-3 and 5-4 show the function of the interface pins in minimum and maximum modes. *Figure 5-10* shows the location of each port's status information when maximum mode is selected. This may be compared with the connection diagram *(Figure 5-9)*.

Immediately following the MLOAD Operation (when the $\overline{\text{MLOAD}}$ pin transitions to a high logic state), the display logic performs an LED test operation. This operation lasts one second and while it is in effect all of the utilized LEDs will blink on. Thus an installation engineer is able to test the operation of the display by forcing the LERIC into a reset cycle ($\overline{\text{MLOAD}}$ forced low). The rising edge on the $\overline{\text{MLOAD}}$ pin starts the LED test cycle. **During the LED test cycle the LERIC does not perform packet repetition operations.**

The status display possesses a capability to lengthen the time an LED is active. At the end of the repetition of a packet, the display is frozen showing the current activity. This freezing lasts for 30 ms or until a subsequent packet is repeated. Thus at low levels of packet activity the display stretches activity information to make it discernable to the human eye. At high traffic rates the relative brightness of the LEDs indicates those segments with high or low activity.

TABLE 5-3. Status Display Pin Functions in Minimum Mode

Signal Pin Name	Mnemonic	Function in MINIMUM MODE
D0	ACOL	Provides status information indicating if there is a collision occurring on one of the segments attached to this LERIC.
D1	AREC	Provides status information indicating if one of this LERIC's ports is receiving a data or collision packet from a segment attached to this LERIC.
D2	JAB	Provides status information indicating that the LERIC has experienced a jabber protect condition.
D3	APART	Provides status information indicating if one of the LERIC's segments is partitioned.
D(7:4)		No operation
$\overline{\text{STR}}$		This signal is the latch enable for the 374 type latch.

Note: ACOL = Any Port Collision
AREC = Any Port Reception
JAB = Any Port Jabbering
APART = Port Partitioned

5.0 Functional Description (Continued)

TABLE 5-4. Status Display Pin Functions in Maximum Mode

Signal Pin Name	Function in MAXIMUM MODE
D0	Provides status information concerning the Link Integrity status of 10BASE-T segments. This signal should be connected to the data inputs of the chosen pair of 74LS259 latches.
D1	Provides status information indicating if there is a collision occurring on one of the segments attached to this LERIC. This signal should be connected to the data inputs of the chosen pair of 74LS259 latches.
D2	Provides status information indicating if one of this LERIC's ports is receiving data or a collision packet from its segment. This signal should be connected to the data inputs of the chosen pair of 74LS259 latches.
D3	Provides status information indicating that the LERIC has experienced a jabber protect condition. Additionally, it denotes which of its ports are partitioned. This signal should be connected to the data inputs of the chosen pair of 74LS259 latches.
D4	Provides status information indicating if one of this LERIC's ports is receiving data of inverse polarity. This status output is only valid if the port is configured to use its internal 10BASE-T transceiver. The signal should be connected to the data inputs of the chosen pair of 74LS259 latches.
D(7:5)	These signals provide the repeater port address corresponding to the data available on D(4:0).
$\overline{STR}$	This signal is the latch enable for the 74LS259 latches.

5.0 Functional Description (Continued)

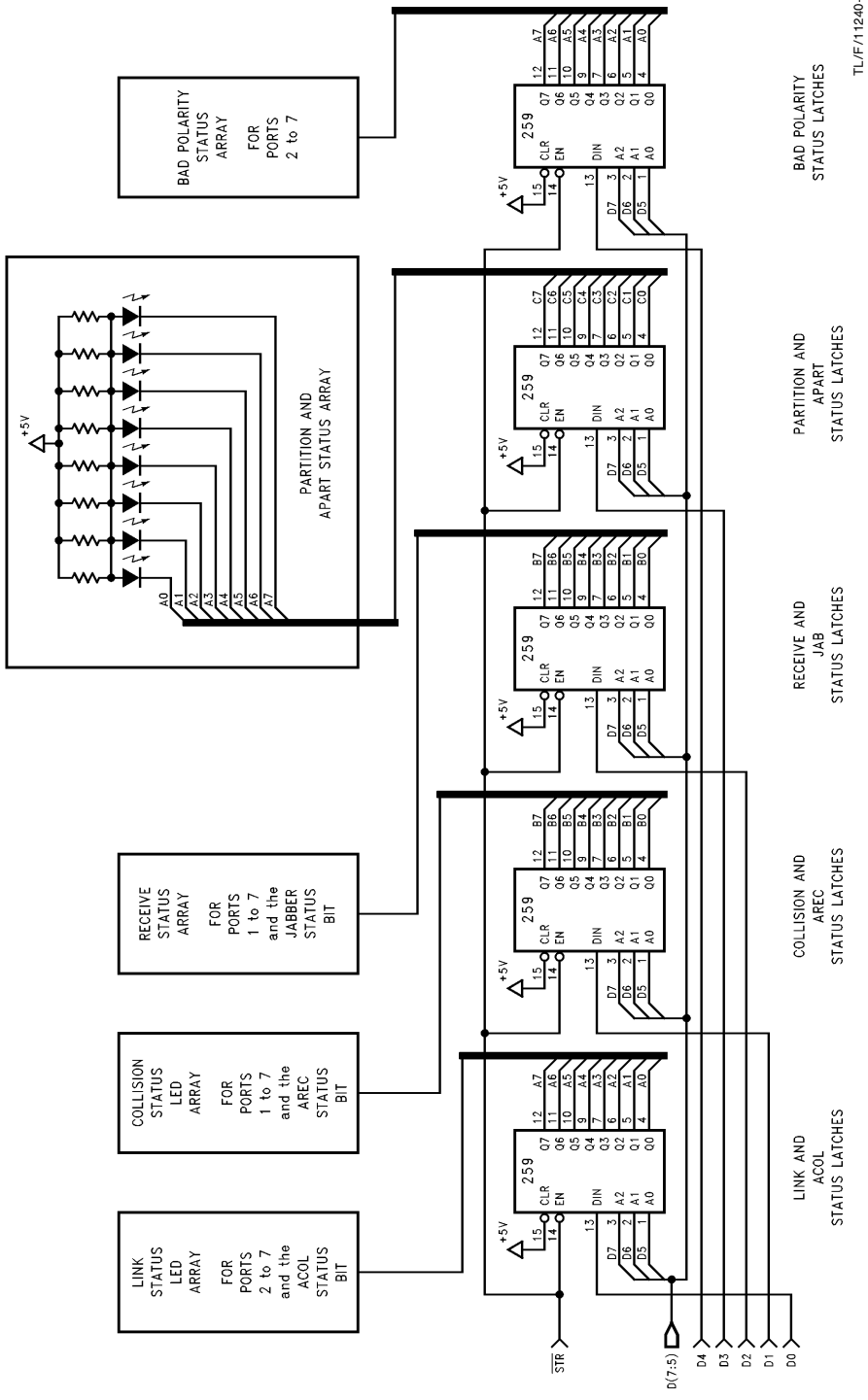


FIGURE 5-9. Maximum Mode LED Display (All Available Status Bits Used)

5.0 Functional Description (Continued)

	74LS259 Latch Inputs							
259 Output	Q0	Q1	Q2	Q3	Q4	Q5	Q6	A7
259 Addr S(2−0)	000	001	010	011	100	101	110	111
LERIC Port Number		1 (AUI)	2	3	4	5	6	7
LERIC D0	ACOL		LINK	LINK	LINK	LINK	LINK	LINK
LERIC D1	AREC	COL	COL	COL	COL	COL	COL	COL
LERIC D2	JAB	REC	REC	REC	REC	REC	REC	REC
LERIC D3	APART	PART	PART	PART	PART	PART	PART	PART
LERIC D4			BDPOL	BDPOL	BDPOL	BDPOL	BDPOL	BDPOL

Note: This shows the LED Output Functions for the LED Drivers when 74LS259s are used.
ACOL = Any Port Collision, AREC = Any Port Reception, JAB = Any Port Jabbering,
LINK = Port Link, COL = Port Collision, REC = Port Reception, PART = Port Partitioned,
BDPOL = Bad (inverse) Polarity of received data

FIGURE 5-10. Maximum Mode LED Definitions

Description of Data Freeze Strobe (DFS) Pin Operation

DFS has been implemented to assist the user to provide partial hub management statistics on a per packet per port basis. The DFS signal is asserted, active high, at the end of the transmission of each packet, and the status of that packet is frozen on the LEDs until the beginning of the next received packet or for a maximum of 30 ms as is shown in *Figure 5-11*.

The DFS signal can be used to latch the LED information into a shared buffer which acts as an external flag register, and can be used as a mechanism to trap events.

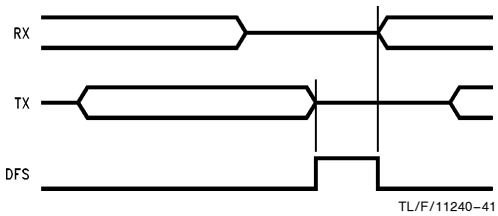


FIGURE 5-11. DFS Operation

Processor Access Cycles

Access to the LERIC's on-chip registers is made via its processor interface. This utilizes a conventional non-multiplexed address (four bit) and data (four bit) bus. This bus is also used to provide data and address information to off chip LED display latches during display update cycles. While performing these cycles the LERIC behaves as a master of its data bus. Consequently a TRI-STATE bi-directional bus transceiver (e.g., 74LS245) must be placed between the LERIC and any processor bus. Internally each of the LERIC's registers is 8 bits, however there are four bits of data pins (D(3:0)). Each register is accessed on a nibble basis (4 bits at a time). D(7) of the address pins D(7:4) selects the upper and lower nibbles as described in Section 7.

To access the LERIC's registers, the processor requests a register access by asserting the read ($\overline{RD}$) or write ($\overline{WR}$) input strobes. The LERIC responds by finishing any current display update cycle and asserts the TRI-STATE buffer enable signal ($\overline{BUFEN}$). If the processor cycle is a write cycle then the LERIC's buffers are disabled to prevent contention. In order to interface to the LERIC a PAL device may be used to perform the following operations:

1. Generate the LERIC's read and write strobes,
2. Control the direction signal for the 74LS245.

An example of the processor and display interfaces is shown in *Figure 5-12*.

5.0 Functional Description (Continued)

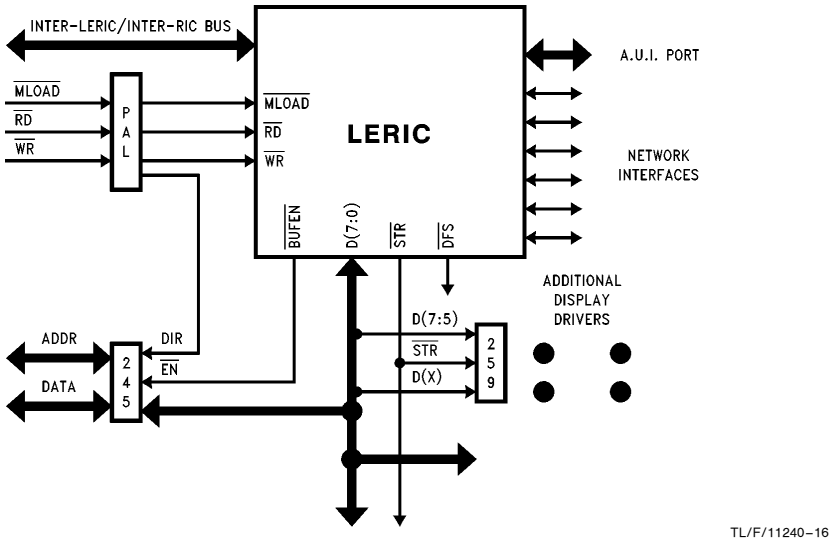


FIGURE 5-12. Processor Connection Diagram

6.0 Port Block Functions

The LERIC has 7 port logic blocks (one for each network connection). In addition to the packet repetition operations already described, the port block performs two other functions:

1. The physical connection to the network segment (transceiver function).
2. It provides a means to protect the network from malfunctioning segments (segment partition).

Each port has its own status and configuration register. This register allows the user to determine the current status of the port and configure a number of port specific functions.

6.1 TRANSCEIVER FUNCTIONS

The LERIC may connect to network segments in three ways:

1. Over AUI cable to transceiver boxes (Port 1)
2. Directly to board mounted transceivers.
3. To twisted pair cable via a simple interface.

The first method is only supported by LERIC Port 1 (the AUI port). Options (2) and (3) are available on Ports 2 to 7. The selection of the desired option is made at device initialization during the MLOAD operation. The Transceiver Bypass XBYPAS configuration bits are used to determine whether the ports will utilize the on-chip 10BASE-T transceivers or bypass these in favor of external transceivers. Four possible combinations of port utilization are supported (refer to Table 5-2):

1. All ports (2 to 7) use the external Transceiver Interface.
2. Ports 2 and 3 use the external interface, 4 to 7 use the internal 10BASE-T transceivers.
3. Ports 2 to 5 use the external interface, 6 and 7 use the internal 10BASE-T transceivers.
4. All ports (2 to 7) use the internal 10BASE-T transceivers.

10BASE-T Transceiver Operation

The LERIC contains virtually all the digital and analog circuits required for connection to 10BASE-T network segments. The only additional active component is an external driver package. The connection for a LERIC port to a 10BASE-T segment is shown in *Figure 6-1.* The diagram shows the components required to connect one of the LERIC's ports to a 10BASE-T segment (and lists a few module P/Ns and vendors). The major components are the driver package, a member of the 74ACT family, and an integrated filter-transformer-choke module (or discrete combination of these functions).

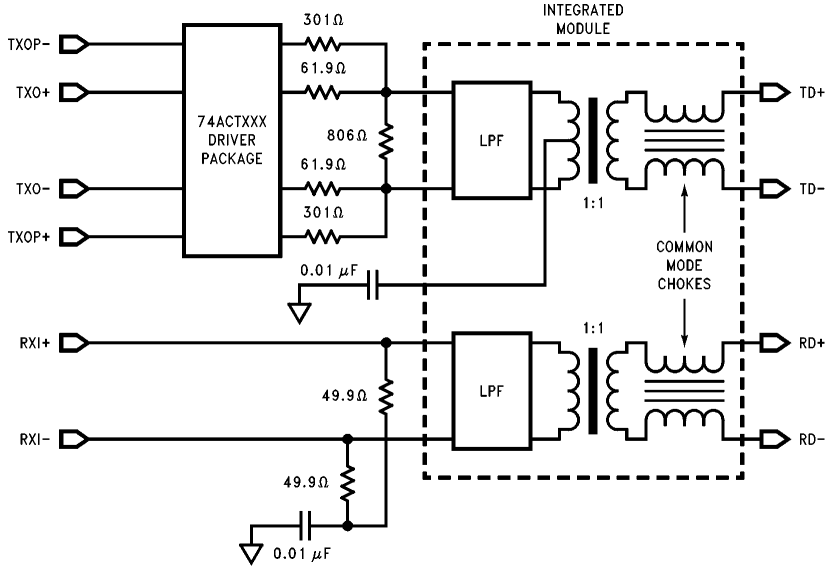
The operation of the 10BASE-T transceiver's logical functions may be modified by software control. The default mode of operation is for the transceivers to transmit and expect reception of link pulses. This may be modified if a logic one is written to the $\overline{\text{GDLNK}}$ bit of a port's status register. The port's transceiver will operate normally but will not transmit link pulses nor monitor their reception. Thus the entry to a link fail state and the associated modification of transceiver operation will not occur.

The on-chip 10BASE-T transceivers automatically detect and correct the polarity of the received data stream. This polarity detection scheme relies upon the polarity of the received link pulses and the end of packet waveform. Polarity detection and correction may be disabled through the MLOAD operation.

External Transceiver Operation

LERIC ports 2 to 7 may be connected to media other than twisted-pair by opting to bypass the on-chip transceivers. When using external transceivers the user must perform collision detection and the other functions associated with an IEEE 802.3 Media Access Unit. *Figure 6-2* shows the connection between a repeater port and a coaxial transceiver using the AUI type interface.

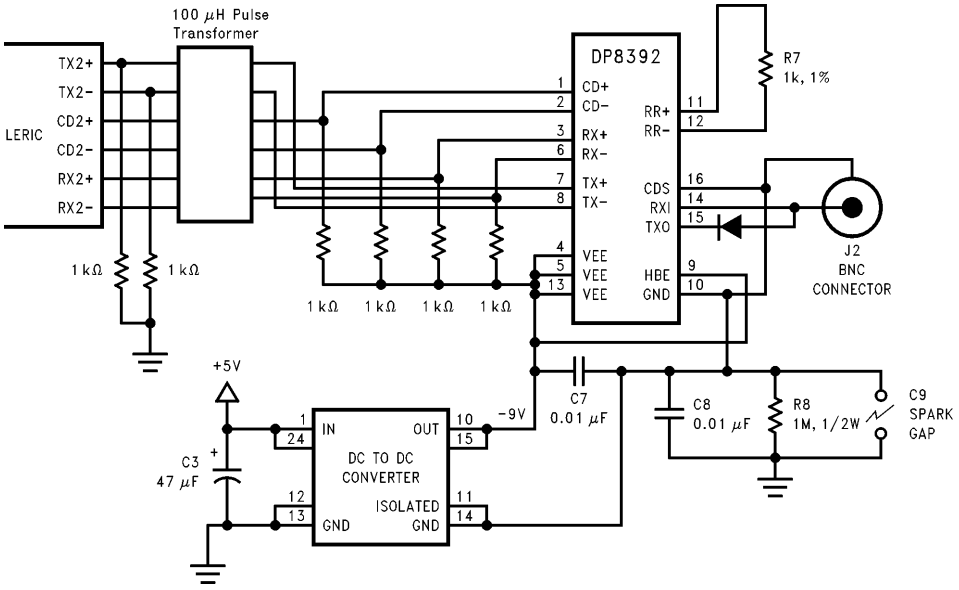
6.0 Port Block Functions (Continued)



TL/F/11240–17

For typical Filter-Transformer-Choke Modules refer to ETHERNET MAGNETIC VENDORS.
In addition to these, the Valor FL1085 is recommended for HCT Drivers.

FIGURE 6-1. Port Connection to a 10BASE-T Segment



TL/F/11240–18

The above diagrams show a LERIC port (numbers 2 to 7) connected to a 10BASE-T and a 10BASE2 segment. The values of any components not indicated above are to be determined.

FIGURE 6-2. Port Connection to a 10BASE2 Segment (AUI type Interface selected)

6.0 Port Block Functions (Continued)

6.2 SEGMENT PARTITION

Each of the LERIC ports has a dedicated state machine to perform the functions defined by the IEEE partition algorithm as shown in *Figure 6-3.* To allow users to customize this algorithm for different applications a number of user selected options are available during device configuration at power up (the MLOAD cycle).

Two options are provided:

1. The value of consecutive counts required to partition a segment (the CCLimit specification) may be set at either 31 or 63 consecutive collisions.
2. The operation of the ports' state machines when reconnecting a segment may also be modified by the user. The Transmit Only $\overline{\text{TXONLY}}$ configuration bit allows the user to prevent segment reconnection unless the reconnecting packet is being sourced by the repeater. In this case the repeater is transmitting on to the segment rather than the segment transmitting when the repeater is idle. The normal mode of reconnection does not differentiate between such packets. The $\overline{\text{TXONLY}}$ configuration bit is input on pin D(5) during the MLOAD cycle. If this option is selected the operation of the state machine branch marked (3) in *Figure 6-3* is affected.

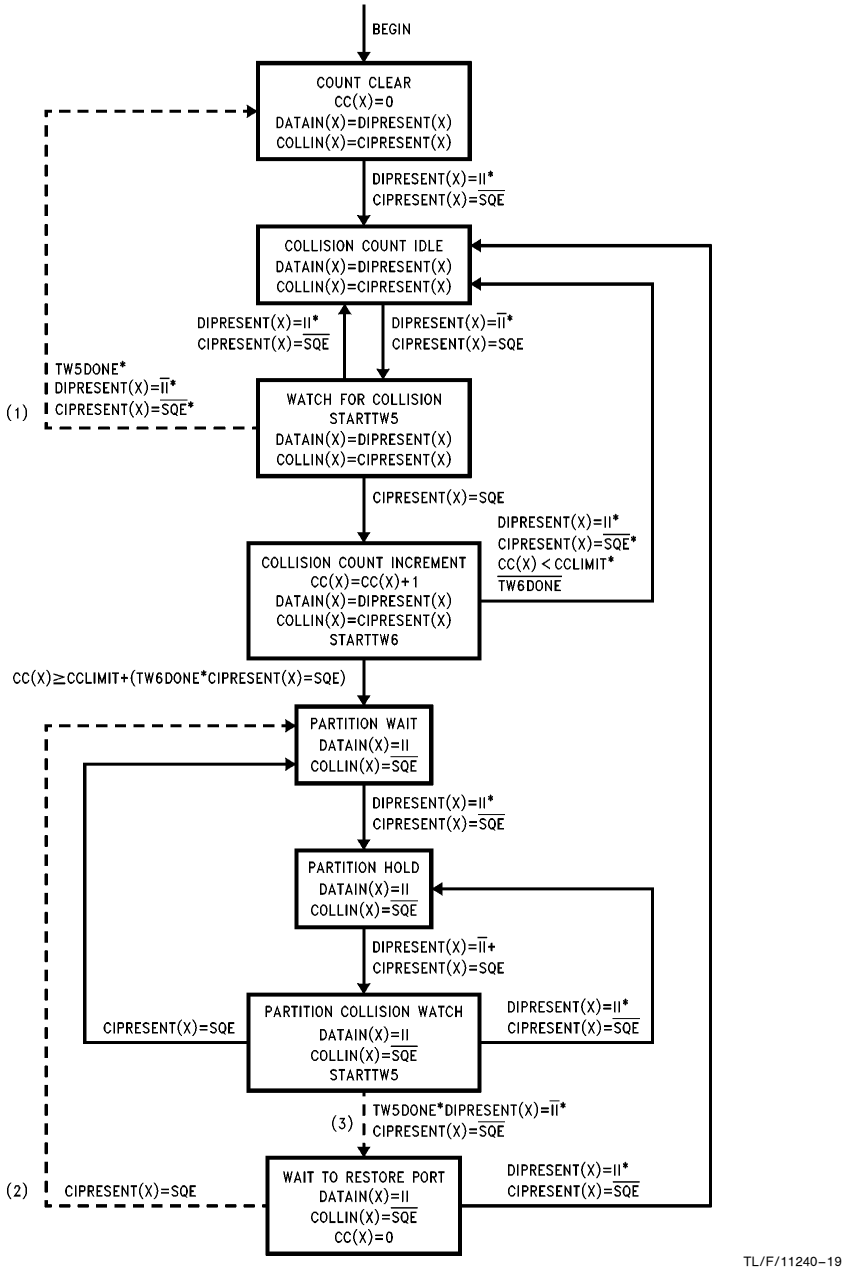
   In addition to the autonomous operation of the partition state machines, the user may reset these state machines. This may be done individually to each port by writing a logic one to the $\overline{\text{PART}}$ bit in its status register. The port's partition state machine and associated counters are reset and the port is reconnected to the network.

6.3 PORT STATUS AND CONFIGURATION REGISTER FUNCTIONS

Each LERIC port has its own status and configuration register. In addition to providing status concerning the port and its network segment the register allows the following operations to be performed upon the port:

1. Port disable. When a port is disabled packet transmission and reception between the port's segment and the rest of the network is prevented.
2. Selection between normal and reduced squelch levels.

6.0 Port Block Functions (Continued)



TL/F/11240–19

FIGURE 6-3. IEEE Segment Partition Algorithm

7.0 LERIC Registers

7.1 LERIC REGISTER ADDRESS MAP

The LERIC's registers may be accessed by applying the required address to the four register address (D(7:4)) input pins. Pin D(7) makes the selection between the upper and lower nibbles of each register. The register map consists of 8 registers as shown in the Register Map in Table 7-1 which is followed by a summary of the register bits shown in Table 7-2. The definitions for these bits are shown in the detailed register definitions on the following pages.

TABLE 7-1. Register Memory Map

Address D(7:4)	Name
0000 1000	LERIC Status Register—Lower Nibble LERIC Status Register—Upper Nibble
0001 1001	Port 1 Status and Configuration Register—Lower Nibble Port 1 Status and Configuration Register—Upper Nibble
0010 1010	Port 2 Status and Configuration Register—Lower Nibble Port 2 Status and Configuration Register—Upper Nibble
0011 1011	Port 3 Status and Configuration Register—Lower Nibble Port 3 Status and Configuration Register—Upper Nibble
0100 1100	Port 4 Status and Configuration Register—Lower Nibble Port 4 Status and Configuration Register—Upper Nibble
0101 1101	Port 5 Status and Configuration Register—Lower Nibble Port 5 Status and Configuration Register—Upper Nibble
0110 1110	Port 6 Status and Configuration Register—Lower Nibble Port 6 Status and Configuration Register—Upper Nibble
0111 1111	Port 7 Status and Configuration Register—Lower Nibble Port 7 Status and Configuration Register—Upper Nibble

Register Array Bit Map

Address D(7:4)	D(3)	D(2)	D(1)	D(0)
0000 1000	$\overline{\text{PART}}$ Resv	$\overline{\text{JAB}}$ Resv	$\overline{\text{AREC}}$ Resv	$\overline{\text{ACOL}}$ Resv
0001 1001	$\overline{\text{PART}}$ DISPT	$\overline{\text{REC}}$ Resv	$\overline{\text{COL}}$ Resv	$\overline{\text{GDLNK}}$ Resv
0010 1010	$\overline{\text{PART}}$ DISPT	$\overline{\text{REC}}$ Resv	$\overline{\text{COL}}$ POL	$\overline{\text{GDLNK}}$ $\overline{\text{SQRL}}$
0011 1011	$\overline{\text{PART}}$ DISPT	$\overline{\text{REC}}$ Resv	$\overline{\text{COL}}$ POL	$\overline{\text{GDLNK}}$ SQL
0100 1100	$\overline{\text{PART}}$ DISPT	$\overline{\text{REC}}$ Resv	$\overline{\text{COL}}$ POL	$\overline{\text{GDLNK}}$ SQL
0101 1101	$\overline{\text{PART}}$ DISPT	$\overline{\text{REC}}$ Resv	$\overline{\text{COL}}$ POL	$\overline{\text{GDLNK}}$ SQL
0110 1110	$\overline{\text{PART}}$ DISPT	$\overline{\text{REC}}$ Resv	$\overline{\text{COL}}$ POL	$\overline{\text{GDLNK}}$ SQL
0111 1111	$\overline{\text{PART}}$ DISPT	$\overline{\text{REC}}$ Resv	$\overline{\text{COL}}$ POL	$\overline{\text{GDLNK}}$ SQL

7.0 LERIC Registers (Continued)

7.2 LERIC STATUS REGISTER

This register contains real time information concerning the operation of the LERIC.

D(3)	D(2)	D(1)	D(0)	D(3)	D(2)	D(1)	D(0)
Resv	Resv	Resv	Resv	$\overline{\text{APART}}$	$\overline{\text{JAB}}$	$\overline{\text{AREC}}$	$\overline{\text{ACOL}}$

Symbol	Bit	R/W	Description
$\overline{\text{ACOL}}$	D(0)	R	Any Collisions 0: A collision is occurring at one or more of the LERIC's ports 1: No collisions
$\overline{\text{AREC}}$	D(1)	R	Any Receive 0: One of the LERIC's ports is the current packet or collision receiver 1: No packet or collision reception within this LERIC
$\overline{\text{JAB}}$	D(2)	R	Jabber Protect 0: The LERIC has been forced into jabber protect state by one of its ports or by another port on the Inter-LERIC bus (operations) 1: No jabber protect conditions exist
$\overline{\text{APART}}$	D(3)	R	Any Partition 0: One or more ports are partitioned 1: No ports are partitioned
Resv	D(0)	R	Reserved for future use Value set at logic one
Resv	D(1)	R	Reserved for future use Value set at logic one
Resv	D(2)	R	Reserved for future use Value set at logic one
Resv	D(3)	R	Reserved for future use Value set at logic one

7.0 LERIC Registers (Continued)

7.3 PORT STATUS AND CONFIGURATION REGISTERS

D(3)	D(2)	D(1)	D(0)	D(3)	D(2)	D(1)	D(0)
DISPT	Resv	POL	SQL	$\overline{\text{PART}}$	$\overline{\text{REC}}$	$\overline{\text{COL}}$	$\overline{\text{GDLNK}}$

Symbol	Bit	R/W	Description
$\overline{\text{GDLNK}}$	D(0)	R/W	Good Link 0: Link pulses are being received by the port 1: Link pulses are not being received by the port logic **Note:** Writing a 1 to this bit will cause the 10BASE-T transceiver not to transmit or monitor the reception of link pulses. If the internal 10BASE-T transceivers are not selected or if port 1 (AUI port) is read, then this bit is undefined.
$\overline{\text{COL}}$	D(1)	R	Collision 0: A collision is happening or has occurred during the current packet 1: No collisions have occurred as yet during this packet
$\overline{\text{REC}}$	D(2)	R	Receive 0: This port is now or has been the receive source of packet or collision information for the current packet. 1: This port has not been the receive source during the current packet
$\overline{\text{PART}}$	D(3)	R/W	Partition 0: This port is partitioned 1: This port is not partitioned Writing a logic one to this bit forces segment reconnection and partition state machine reset. Writing a zero to this bit has no effect.
SQL	D(0)	R/W	Squelch Level 0: Port operates with normal IEEE receive squelch level 1: Port operates with reduced receive squelch levels **Note:** This bit has no effect when the external transceiver is selected.
POL	D(1)	R	Polarity 0: Polarity is not inverted 1: Polarity is inverted
Resv	D(2)	R	‘‘Reserved’’ ‘‘Value set to logic zero’’
DISPT	D(3)	R/W	Disable Port 0: Port operates as defined by repeater operations 1: All port activity is prevented

8.0 Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	0.5V to 7.0V
DC Input Voltage (V_{IN})	−0.5V to V_{CC} + 0.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	1.5W
Lead Temperature (T_L) (Soldering, 10 Seconds)	260°C
ESD Rating (R_{ZAP} = 1.5k, C_{ZAP} = 120 pF)	1.5 kV

9.0 DC Specifications T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified

Symbol	Description	Conditions	Min	Max	Units
PROCESSOR, LED, TWISTED-PAIR PORTS AND INTER-LERIC INTERFACES					
V_{OH}	Minimum High Level Output Voltage	I_{OH} = −8 mA	3.5		V
V_{OL}	Minimum Low Level Output Voltage	I_{OL} = 8 mA		0.4	V
V_{IH}	Minimum High Level Input Voltage		2.0		V
V_{IL}	Maximum Low Level Input Voltage			0.8	V
I_{IN}	Input Current	V_{IN} = V_{CC} or GND	−1.0	1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND	−10	10	μA
I_{CC}	Average Supply Current	V_{IN} = V_{CC} or GND V_{CC} = 5.25V		250	mA
AUI (PORT 1)					
V_{OD}	Differential Output Voltage (TX±)	78Ω Termination and 270Ω Pulldowns	±550	±1200	mV
V_{OB}	Differential Output Voltage Imbalance (TX±)	78Ω Termination and 270Ω Pulldowns		40 mV Typical	
V_U	Undershoot Voltage (TX±)	78Ω Termination and 270Ω Pulldowns		80 mV Typical	
V_{DS}	Differential Squelch Threshold (RX±, CD±)		−175	−300	mV
V_{CM}	Differential Input Common Mode Voltage (RX±, CD±) (Note 1)		0	5.5	V

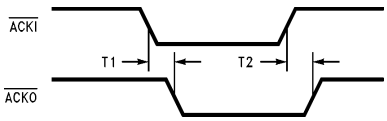
9.0 DC Specifications $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified (Continued)

Symbol	Description	Conditions	Min	Max	Units
PSEUDO AUI (PORTS 2–7)					
V_{POD}	Differential Output Voltage (TX±)	270Ω Termination and 1 kΩ Pulldowns	±450	±1200	mV
V_{POB}	Differential Output Voltage Imbalance (TX±)	270Ω Termination and 1 kΩ Pulldowns		40 mV Typical	
V_{PU}	Undershoot Voltage (TX±)	270Ω Termination and 1 kΩ Pulldowns		80 mV Typical	
V_{PDS}	Differential Squelch Threshold (RX±, CD±)		−175	−300	mV
V_{PCM}	Differential Input Common Mode Voltage (RX±, CD±) (Note 1)		0	5.5	V
TWISTED-PAIR (PORTS 2–7)					
V_{RON}	Minimum Receive Squelch Threshold: Normal Mode Reduced Mode		 ±300 ±175	 ±585 ±300	 mV mV

Note 1: This parameter is guaranteed by design and is not tested.

10.0 Switching Characteristics

PORT ARBITRATION TIMING



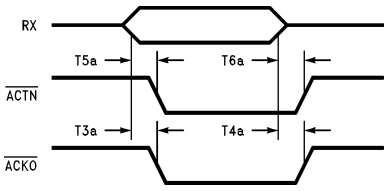
TL/F/11240–20

Symbol	Number	Parameter	Min	Max	Units
ackilackol	T1	$\overline{ACKI}$ Low to $\overline{ACKO}$ Low		26	ns
ackihackoh	T2	$\overline{ACKI}$ High to $\overline{ACKO}$ High		23	ns

Note: Timing valid with no receive or collision activities.

RECEIVE TIMING—AUI PORTS

Receive activity propagation start up and end delays for ports in **non** 10BASE-T mode



TL/F/11240–21

Symbol	Number	Parameter	Min	Max	Units
rxaackol	T3a	RX Active to $\overline{ACKO}$ Low		66	ns
rxiackoh	T4a	RX Inactive to $\overline{ACKO}$ High (Note 1)		235	ns
rxaactnl	T5a	RX Active to $\overline{ACTN}$ Low		75	ns
rxiactnh	T6a	RX Inactive to $\overline{ACTN}$ High (Note 1)		235	ns

Note: $\overline{ACKI}$ assumed high

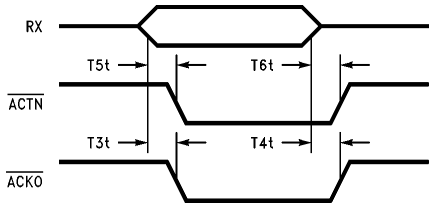
Note 1: This time includes EOP.

Note 2: This parameter assumes squelch triggers on negative edge of RX data.

10.0 Switching Characteristics (Continued)

RECEIVE TIMING-10BASE-T PORTS

Receive activity propagation start up and end delays for ports in 10BASE-T mode



TL/F/11240–22

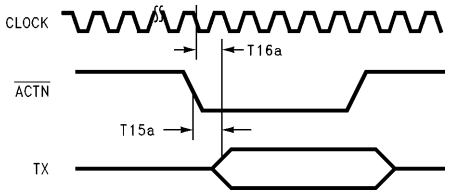
Symbol	Number	Parameter	Min	Max	Units
rxaackol	T3t	RX Active to $\overline{\text{ACKO}}$ Low		300	ns
rxiackoh	T4t	RX Inactive to $\overline{\text{ACKO}}$ High (Note 1)		280	ns
rxaactnl	T5t	RX Active to $\overline{\text{ACTN}}$ Low		300	ns
rxiactnh	T6t	RX Inactive to $\overline{\text{ACTN}}$ High (Note 1)		280	ns

Note: $\overline{\text{ACKI}}$ assumed high.

Note 1: This time includes EOP.

TRANSMIT TIMING—AUI PORTS

Transmit activity propagation start up and end delays for ports in **non** 10BASE-T mode



TL/F/11240–23

Symbol	Number	Parameter	Min	Max	Units
actnltxa	T15a	$\overline{\text{ACTN}}$ Low to TX Active		675	ns
clkitxa	T16a	CLOCK in to TX Active (Note 1)		45	ns

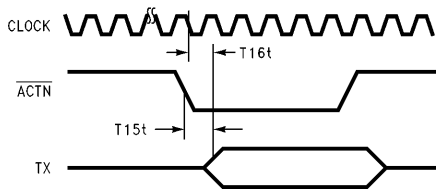
Note: $\overline{\text{ACKI}}$ assumed high.

Note 1: Measurement from previous falling edge of the clock.

10.0 Switching Characteristics (Continued)

TRANSMIT TIMING—10BASE-T PORTS

Receive activity propagation start up and end delays for ports in 10BASE-T mode



TL/F/11240–24

Symbol	Number	Parameter	Min	Max	Units
actnltxa	T15t	$\overline{\text{ACTN}}$ Low to TX Active		790	ns
clkitxa	T16t	CLOCK in to TX Active (Note 1)		45	ns

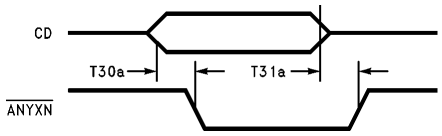
Note: $\overline{\text{ACKI}}$ assumed high.

Note 1: Clock not drawn to scale. In this measurement, falling edge of the clock for even ports and rising edge of the clock for odd ports are considered.

COLLISION TIMING—AUI PORTS

Collision activity propagation start up and end delays for ports in **non** 10BASE-T mode

TRANSMIT COLLISION TIMING



TL/F/11240–25

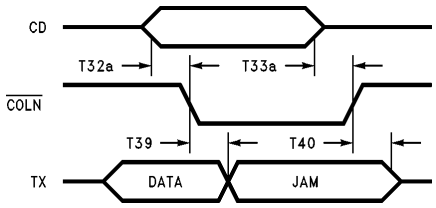
Symbol	Number	Parameter	Min	Max	Units
cdaanyxnl	T30a	CD Active to $\overline{\text{ANYXN}}$ Low		85	ns
cdianyxnh	T31a	CD Inactive to $\overline{\text{ANYXN}}$ High (Notes 1, 2)		285	ns

Note 1: TX collision extension has already been performed and no other port is driving $\overline{\text{ANYXN}}$.

Note 2: Includes TW2.

10.0 Switching Characteristics (Continued)

RECEIVE COLLISION TIMING



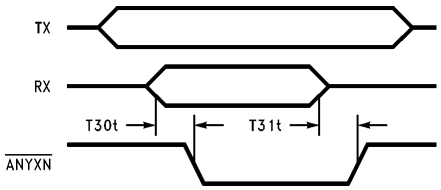
TL/F/11240–26

Symbol	Number	Parameter	Min	Max	Units
cdacolna	T32a	CD Active to $\overline{\text{COLN}}$ Low		75	ns
cdicolni	T33a	CD Inactive to $\overline{\text{COLN}}$ High		215	ns
colnljs	T39	$\overline{\text{COLN}}$ Low to Start of JAM		400	ns
colnhje	T40	$\overline{\text{COLN}}$ High to End of JAM(Note 1)		585	ns

Note 1: Reception ended before $\overline{\text{COLN}}$ goes high.

COLLISION TIMING—10BASE-T PORTS

Collision activity propagation start up and end delays for ports in 10BASE-T mode



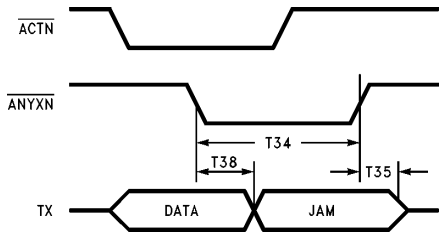
TL/F/11240–27

Symbol	Number	Parameter	Min	Max	Units
colaanyl	T30t	Collision Active to $\overline{\text{ANYXN}}$ Low		800	ns
colianyh	T31t	Collision Inactive to $\overline{\text{ANYXN}}$ High (Note 1)		450	ns

Note 1: TX collision extension has already been performed and no other port is asserting $\overline{\text{ANYXN}}$.

10.0 Switching Characteristics (Continued)

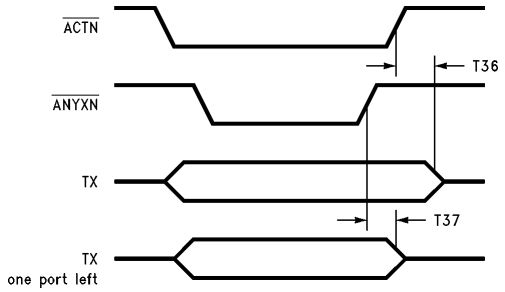
COLLISION TIMING—ALL PORTS



TL/F/11240–28

Symbol	Number	Parameter	Min	Max	Units
anylmin	T34	$\overline{\text{ANYXN}}$ Low Time	96		bits
anyhtxai	T35	$\overline{\text{ANYXN}}$ High to TX to All Inactive	20	370	ns
anylsj	T38	$\overline{\text{ANYXN}}$ Low to Start of JAM		565	ns

COLLISION TIMING—ALL PORTS



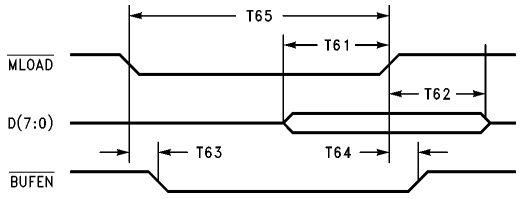
TL/F/11240–29

Symbol	Number	Parameter	Min	Max	Units
actnhtxi	T36	$\overline{\text{ACTN}}$ High to TX Inactive		410	ns
anyhtxoi	T37	$\overline{\text{ANYXN}}$ High to TX ''One Port Left'' Inactive	20	200	ns

Note: 96 bits of JAM have already been propagated.

10.0 Switching Characteristics (Continued)

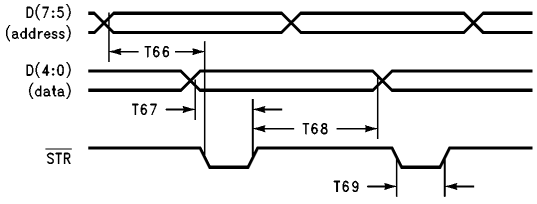
RESET TIMING



TL/F/11240–30

Symbol	Number	Parameter	Min	Max	Units
resdats	T61	Data Setup	20		ns
resdath	T62	Data Hold	20		ns
reslbufl	T63	$\overline{\text{MLOAD}}$ Low to $\overline{\text{BUFEN}}$ Low		35	ns
reshbufh	T64	$\overline{\text{MLOAD}}$ High to $\overline{\text{BUFEN}}$ High		35	ns
resw	T65	$\overline{\text{MLOAD}}$ Width	800		ns

LED STROBE TIMING

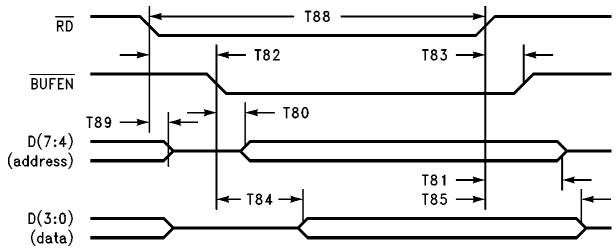


TL/F/11240–31

Symbol	Number	Parameter	Min	Max	Units
stradrs	T66	Strobe Address Setup	70	100	ns
strdats	T67	Strobe Data Setup	35	55	ns
strdath	T68	Strobe Data Hold	145	165	ns
strw	T69	Strobe Width	30	65	ns

10.0 Switching Characteristics (Continued)

REGISTER READ TIMING

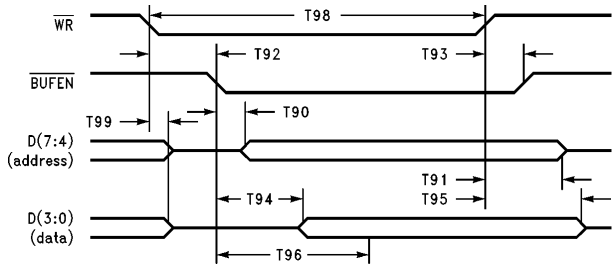


TL/F/11240–32

Symbol	Number	Parameter	Min	Max	Units
rdadrs	T80	Address Setup from $\overline{\text{BUFEN}}$ Low	0	85	ns
rdadrh	T81	Address Hold after $\overline{\text{RD}}$ High	0		ns
rdlbufl	T82	$\overline{\text{RD}}$ Low to $\overline{\text{BUFEN}}$ Low	80	355	ns
rdhbufh	T83	$\overline{\text{RD}}$ High to $\overline{\text{BUFEN}}$ High		35	ns
bufldatv	T84	$\overline{\text{BUFEN}}$ Low to Data Valid		190	ns
rddath	T85	Read Data Hold	60		ns
rdw	T88	$\overline{\text{RD}}$ Width	650		ns
rdtr	T89	$\overline{\text{RD}}$ Low to D(7:4) TRI-STATE	80	355	ns

Note: Minimum high time between read/write cycles is 100 ns.

REGISTER WRITE TIMING



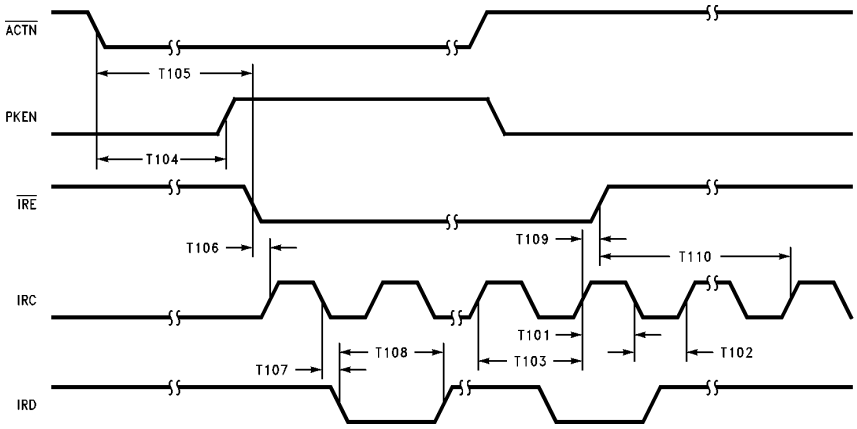
TL/F/11240–33

Symbol	Number	Parameter	Min	Max	Units
wradrs	T90	Address Setup from $\overline{\text{BUFEN}}$ Low	0	14	ns
wradrh	T91	Address Hold after $\overline{\text{WR}}$ High	0		ns
wrlbufl	T92	$\overline{\text{WR}}$ Low to $\overline{\text{BUFEN}}$ Low	80	355	ns
wrhbufh	T93	$\overline{\text{WR}}$ High to $\overline{\text{BUFEN}}$ High		35	ns
wradatv	T94	$\overline{\text{BUFEN}}$ Low to Data Valid		160	ns
wrdath	T95	Write Data Hold	0		ns
wrdatr	T96	$\overline{\text{BUFEN}}$ Low to Data Latched	245		ns
wrw	T98	$\overline{\text{WR}}$ Width	650		ns
wrtr	T99	$\overline{\text{WR}}$ Low to D(7:0) TRI-STATE	80	355	ns

Note: Minimum high time between read/write cycles is 100 ns.

10.0 Switching Characteristics (Continued)

INTER-LERIC BUS OUTPUT TIMING

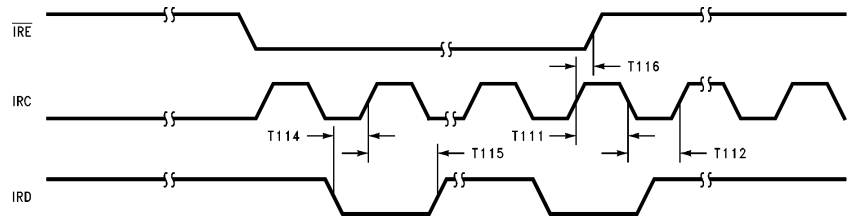


TL/F/11240–34

Symbol	Number	Parameter	Min	Max	Units
ircoh	T101	IRC Output High Time	40	60	%
ircol	T102	IRC Output Low Time	40	60	%
ircoc	T103	IRC Output Cycle Time	90	110	ns
actndapkena	T104	ACTNd Active to PKEN Active (Note 1)	500		ns
actnolireol	T105	$\overline{\text{ACTN}}$ Output Low to $\overline{\text{IRE}}$ Output Low	500		ns
ireolirca	T106	$\overline{\text{IRE}}$ Output Low to First Rising Edge of IRC		1.8	μs
irdov	T107	IRD Output Valid from IRC		10	ns
irdos	T108	IRD Output Stable Valid Time	90		ns
ircohireh	T109	IIRC Output High to $\overline{\text{IRE}}$ High	30	70	ns
ircclks	T110	Number of IRCs after $\overline{\text{IRE}}$ High	5	5	clocks

Note 1: This parameter applies to DP83956 only.

INTER-LERIC BUS INPUT TIMING



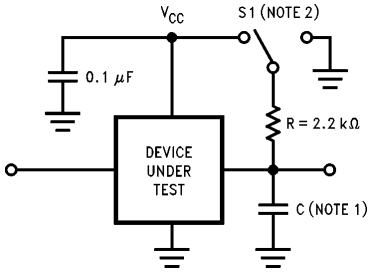
TL/F/11240–35

Symbol	Number	Parameter	Min	Max	Units
ircih	T111	IRC Input High Time	20		ns
ircil	T112	IRC Input Low Time	20		ns
irdisirc	T114	IRD Input Setup to IRC	5		ns
irdihirc	T115	IRD Input Hold from IRC	10		ns
ircihireh	T116	IRC Input High to $\overline{\text{IRE}}$ High	25	75	ns

11.0 AC Timing Test Conditions

All specifications are valid only if the mandatory isolation is employed and all differential signals are taken to be at AUI side of the pulse transormer.

Input Pulse Levels (TTL/CMOS)	GND to 3.0V
Input Rise and Fall Times (TTL/CMOS)	5 ns
Input and Output Reference Levels (TTL/CMOS)	1.5V
Input Pulse Levels (Diff.)	−350 mV to −1315 mV
Input and Output Reference Levels (Diff.)	50% Point of the Differential
TRI-STATE Reference Levels	Float (Δ) ±0.5V
Output Load (See *Figure* Below)	



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Note 1: 100 pF, include scope and jig capacitance.

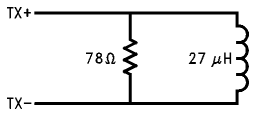
Note 2: S1 = Open for timing tests for push pull outputs.
S1 = V_{CC} for V_{OL} test.
S1 = GND for V_{OH} test.
S1 = V_{CC} for High Impedance to active low and active low to High Impedance measurements.
S1 = GND for High Impedance to active high and active high to High Impedance measurements.

Capacitance $T_A = 25°C$, f = 1 MHz

Symbol	Parameter	Typ	Units
C_{IN}	Input Capacitance	7	pF
C_{OUT}	Output Capacitance	7	pF

Derating Factor

Output timings are measured with a purely capacitive load for 50 pF. The following correction factor can be used for other loads: $C_L \geq 50\ pF + 0.3\ ns/pF$.



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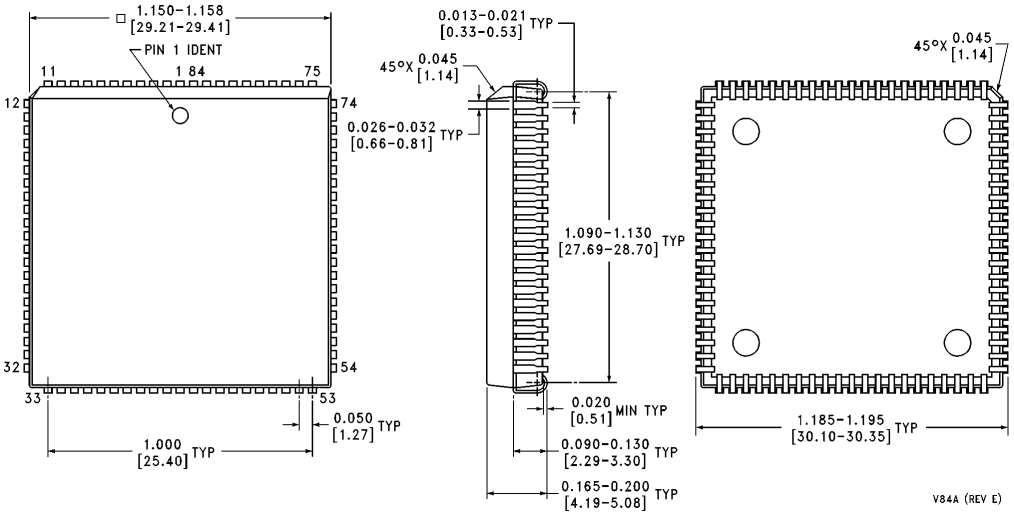
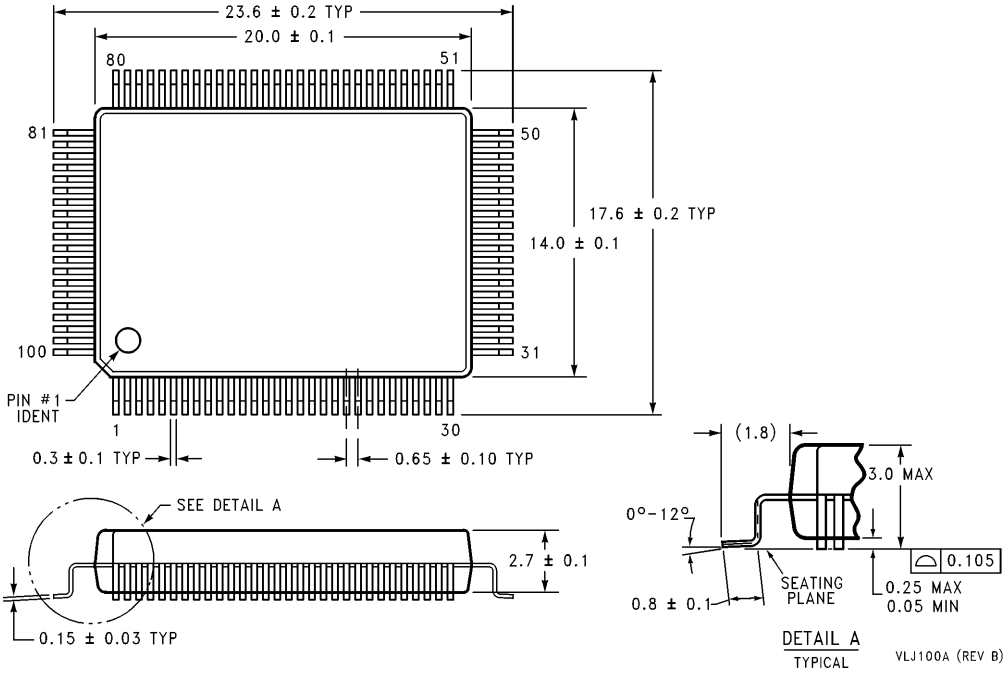
Note: In the above diagram, the TX+ and TX− signals are taken from the AUI side of the isolation (pulse transformer). The pulse transformer used for all testing is the Pulse Engineering PE64103.

Physical Dimensions inches (millimeters)



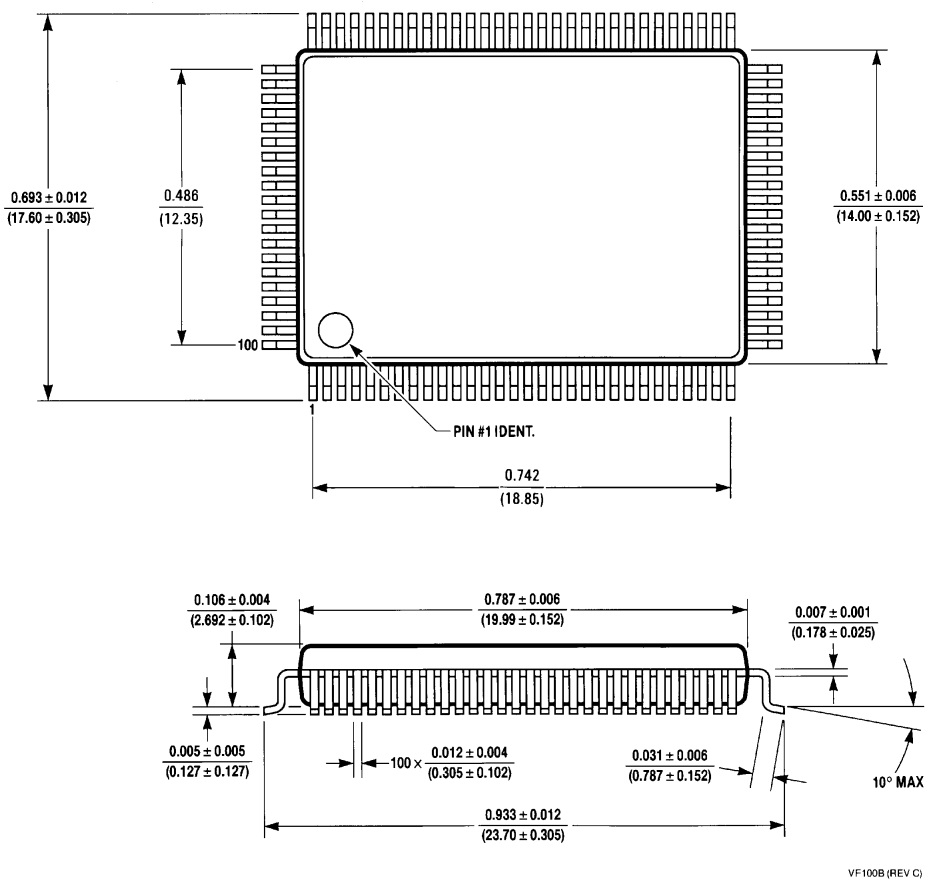
Plastic Chip Carrier (V)
Order Number DP83955AV
NS Package Number V84A

Physical Dimensions inches (millimeters) (Continued)



Plastic Quad Flatpak
Order Number DP83956AVLJ
NS Package Number VLJ100A

Physical Dimensions inches (millimeters) (Continued)



Plastic Quad Flatpak
Order Number DP83956AVLY
NS Package Number VF100B

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